



Gowin PCI Target IP

User Guide

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Revision History

Date	Version	Description
08/30/2019	1.0E	Initial version published.
03/30/2020	1.1E	1100 and 1110 description in PCI Target commands list updated. PCI Target pci_serr_l, pci_perr_l, tg_value description updated.
12/31/2025	1.2E	● Updated 1.2 Related Documents. ● Updated Table 2-2 Resource Utilization to add the information for GW5A-25 devices.

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1 About This Guide

1.1 Purpose

Gowin PCI Target IP user guide aims to help you learn the features and performance, parameter configuration and functional description of Gowin PCI Target IP.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [DS841, GW1NZ series of FPGA Products Data Sheet](#)
- [DS861, GW1NSR series of FPGA Products Data Sheet](#)
- [DS891, GW1NRF series of FPGA Products Data Sheet](#)
- [DS881, GW1NSER series of Bluetooth FPGA Products Data Sheet](#)
- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS981, GW5AT series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1239, GW5AST series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1118, GW5ART series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1 below.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
IP	Intellectual Property
LUT	Look-up Table
PCI	Peripheral Component Interconnect
PCI Target	PCI Target
BAR	Base Address Register

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Overview

This user guide describes PCI Target IP, which provides 33MHz, 32-bit PCI Target solution complying with the local bus specification. It can be used in many applications including telecommunications, embedded systems, high-performance peripheral cards and standards.

Table 2-1 Gowin PCI Target IP Overview

Gowin PCI Target IP	
Logic Resource	See Table 2-2.
Delivered Doc.	
Design Files	Verilog (encryption)
Testing platform	Verilog
Test and Design Flow	
Synthesis Software	GowinSynthesis
Application Software	Gowin Software

Note!

For the devices supported, you can click [here](#) to get the information.

2.1 Features

- Supports 32-bit/33MHz PCI bus
- Supports PCI 2.2 protocol and complies with local bus specification
- Supports a parity bit
- Up to six base address registers
- Supports single cycle read/write and burst read/write
- Supports zero wait state transmission
- Supports an interrupt signal from the backend device to the PCI bus
- Supports parity error signals and system error signals

2.2 Resource Utilization

Gowin PCI Target IP employs Verilog, and different modes use different resources.

The resource utilization with BAR0/BAR1 and 8M base is as shown in

Table 2-2. For the resource utilization of other devices, please refer to the later release information.

Table 2-2 Resource Utilization

LUTs	REGs	Block RAMs	Device Series
252	281	0	GW2A-18
252	281	0	GW1N-9
256	280	0	GW5A-25

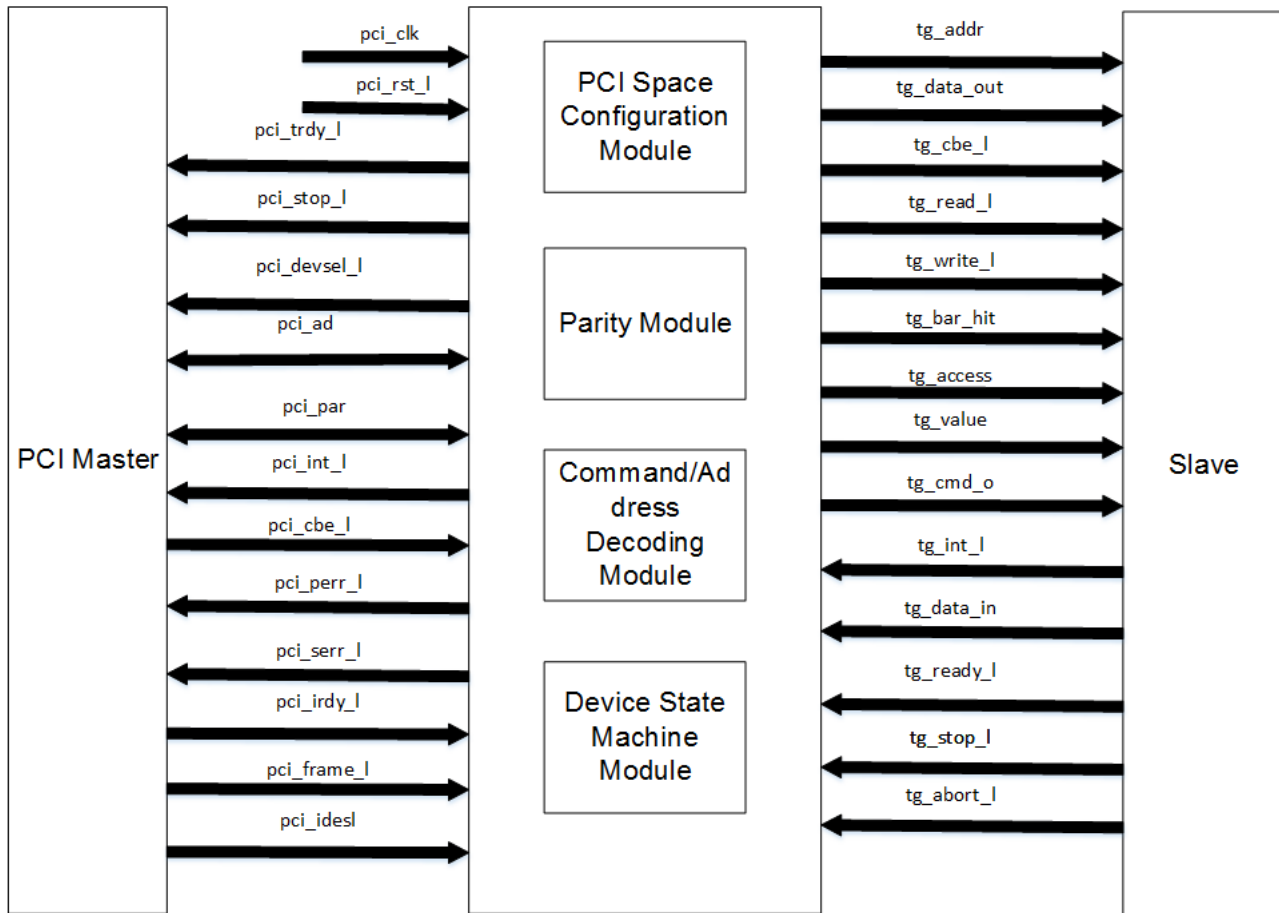
3 Functional Description

Gowin PCI Target IP provides a solution for PCI applications and a 33M, 32-bit customizable PCI Target complying with the local bus specification and PCI 2.2 protocol. It can implement PCI operations: read and write configuration, single cycle read and write, burst read and write, and so on.

3.1 Block Diagram

The block diagram of PCI Target is as shown in Figure 3-1. Since PCI Target is to realize the function of Target, it mainly includes PCI space configuration module, parity module, command/address decoding module and state machine module. The master and backend part shall be subject to specific design.

Figure 3-1 PCI Target Block Diagram



3.2 Module Description

3.2.1 Space Configuration Module

This module implements the logic of PCI Target space configuration. Before read and write operations, configure the space register including device ID, command register, status register, base address register, and so on. PCI Target will complete the corresponding functions with the correct register configuration.

3.2.2 Parity Module

This module is to perform parity of the data address on PCI bus. pci_perr_l and pci_serr_l signals can be configured in the space configuration.

3.2.3 Address/Command Decoding Module

This module realizes the following functions:

1. Control the base address register in space configuration and realize address decoding function.
2. This module will generate "bar_hit[5:0]" signal and send it to the state machine module according to the base selection. This signal is used to indicate which base is currently carrying out data transmission. For example, the 0th bit of "bar_hit[5:0]" will become high and the

remaining are low when base 0 is carrying out data transmission.

3.2.4 State Machine Module

Backend design signals and PCI bus signals almost all pass through the state machine module. This module determines the current working status of PCI Target by judging the status of various signals. For example, the operations of PCI Target include reading and writing data, the termination of data transmission, etc. The module will determine what operations should be performed according to the status of relevant signals.

3.3 PCI Command

The commands supported by Gowin PCI Target IP are shown in Table 3-1.

Table 3-1 PCI Target Commands List

pci_cbe_l	Command	Support or not
0000	Interrupt acknowledge	No
0001	Special Cycle	No
0010	I/O Read	Yes
0011	I/O Write	Yes
0100	Reserved	Reserved
0101	Reserved	Reserved
0110	Memory Read	Yes
0111	Memory Write	Yes
1000	Reserved	Reserved
1001	Reserved	Reserved
1010	Configuration Read	Yes
1011	Configuration Write	Yes
1100	Memory Read Multiple Lines	No
1101	Dual Address Cycle	No
1110	Memory Read One Line	No
1111	Memory Write, invalid	No

3.4 Register Configuration

3.4.1 Register Address Mapping Configuration

The configuration supported by Gowin PCI Target IP is as shown in Table 3-2. The first 64 bytes are called header area, where each field is used to identify the device and enables the device to be controlled in a general way.

Table 3-2 Configuration Space

Device ID	Vendor ID	00h
State register	Command register	04h
Class Code	Revision ID	08h

Reserved				0Ch
BAR 0				10h
BAR 1				14h
BAR 2				18h
BAR 3				1Ch
BAR 4				20h
BAR 5				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Reserved				30h
Reserved				34h
Reserved				38h
Reserved	Reserved	Interrupt Pin	Interrupt Trunk	3Ch

3.4.2 Register Description

Reg00h Device ID and Vendor ID

Reg00h device ID and vendor ID are as shown in Table 3-3.

Table 3-3 Reg00h Device ID and Vendor ID

Location	Naming	Description
31~16	Device ID	This field is used to indicate a specific device and the specific code is assigned by the vendor.
15~0	Vendor ID	This field is used to identify the manufacturer of the device.

Reg04h Command Register and Status Register

The command register is a 16-bit read and write register that provides simple control over the device. It is located at the lower 16-bit address 0x04h and can be used to disable memory and I/O read and write, only allowing read and write configuration. This register also controls the parity error signal and system error signal. Table 6-3 details each command supported by the command register.

Table 3-4 Description of Command Register

Location	Description
0	I/O space control. Control the response to I/O space access. When it is 0, response to I/O space access from device is forbidden. When it is 1, the device is allowed to respond to access to the I/O space.
1	Memory space control. Controls the response to memory space access. When it is 0, response to memory space access from device is forbidden. When it is 1, the device is allowed to respond to access to memory space.
2~5	Reserved
6	Parity error response. This bit is used to control the response to

Location	Description
	parity error from the device. When the bit is 0, the device must ignore any parity error and continue the operation. When the bit is 1, the device must take a response when a parity error is found. The bit must be 0 after reset. Devices with parity must implement the bit, and even if parity is forbidden, still generates parity bit.
7	Reserved
8	System error enable. Used to control system error bit. When the bit is 0, the system error bit is forbidden to work. When the bit is 1, the system error bit is allowed to work
9~11	Reserved

The status register is a 16-bit read and write register that provides function for PCI Target IP and also reports error status. The status register is located at the upper 16 bits of address 0x04h, and the device can decide which bit of the status register to implement, not all bits, according to its own functions. The system has no special requirements on the read operation of this register. The write operation is different because some bits of the register are clearable but unconfigurable. When 1 is written to the clearable but unconfigurable bit, this bit will be cleared. For example, 0000_0100_0000_0000 should be written to the register in order to clear bit 10 without affecting other bits. Table 6-4 details the functions supported by the status register.

Table 3-5 Description of Status Register

Location	Description
0~8	Reserved
9~10	DEVSEL time scale. The two bits represent the time relationship of pci_devsel_I signal. The encoding value represents three address decoding speeds. 00 means fast; 01 means medium; 10 means slow; 11 means reserved. Both bits are read-only. Only slow speed is supported in this design. The specific configuration is shown below. 00 - fast (not supported) 01 -- medium (not supported) 10 - slow 11 - reserved
11	Target abandonment symbol When the target device terminates a transaction by target abandonment, this bit must be set to 1. If the device does not initiate the target abandonment, the bit does not need to be implemented.
12	Reserved
13	Reserved
14	System error enable. When the device sends a system error signal, this bit must be set to 1. When no system error signal will be sent, the device does not have to implement this bit.
15	Parity error symbol. This bit must be 1 when the device detects an error, even if bit 6 in the command register is in a non-enabled state.

Reg08h Class Code and Revision ID

The class code and revision ID are as shown in Table 3-6.

Table 3-6 Class Code and Revision ID

Location	Naming	Description
31~8	Class Code	This field is a 24-bit, read-only, register-level programming interface that identifies the functions of the device. The register includes three segments, each of which takes up one byte. The high bit byte interviews a basic class code at 0x0bh to classify the functions of the device. The medium byte at 0x0ah is called the subclass code, which provides a more precise and detailed classification of the functions of device. The low bit byte at 0x09h identifies a specific register-level programming interface so that device-independent software can interact with the device.
7~0	Revision ID	This field is an 8-bit read-only that specifies a device-specific revision ID. It is selected by the vendor.

Reg10h~24h I/O Space and Memory Space Configuration in BAR

PCI Target supports up to six BARs for Target configuration. In all BARs, bit 0 is read-only and is used to determine whether it is memory space or I/O space. If the bit is 0, it maps to the memory space. And if it is 1, it maps to the I/O address space.

The description of the I/O address space is as shown in Table 3-7, and the bit 0 is equal to 1.

Table 3-7 I/O BAR Description

Location	Description
31~2	Size
1	The reserved bit and the read value must be 0.
0	When the bit is 1, it indicates access to I/O address space.

The memory space description is as shown in Table 3-8, and the bit 0 here is equal to 0.

Table 3-8 Memory Space Description

Location	Description
31~4	Size
3	Prefetching control bit; Prefetching enables at 1 and it is invalid at 0. This bit is only valid when accessing memory space.
2~1	BAR address type. 00-32 bit address space. 01 - reserved 10 – 64-bit address space (Not supported). 11 - reserved

Location	Description
	This design only supports 32 bits.
0	A bit of 0 indicates access to memory space

Reg2Ch Subsystem ID and Subsystem Vendor ID

Reg2Ch subsystem ID and subsystem vendor ID are shown in Table 3-9.

Table 3-9 Subsystem ID and Subsystem Vendor ID

Location	Naming	Description
31~16	Subsystem ID	The subsystem ID is a 16-bit read-only field that further identifies a specific device. This field is defined by the vendor to uniquely identify the product or model.
15~0	Subsystem Vendor ID	The subsystem vendor ID is a 16-bit read-only field that is used to further identify the vendor of the extension board or subsystem.

Reg3Ch Max_Lat, Min_Gnt, Interrupt Pin and Interrupt Trunk

The description of Reg3Ch Max_Lat, Min_Gnt, interrupt pin and interrupt trunk are as shown in Table 3-10.

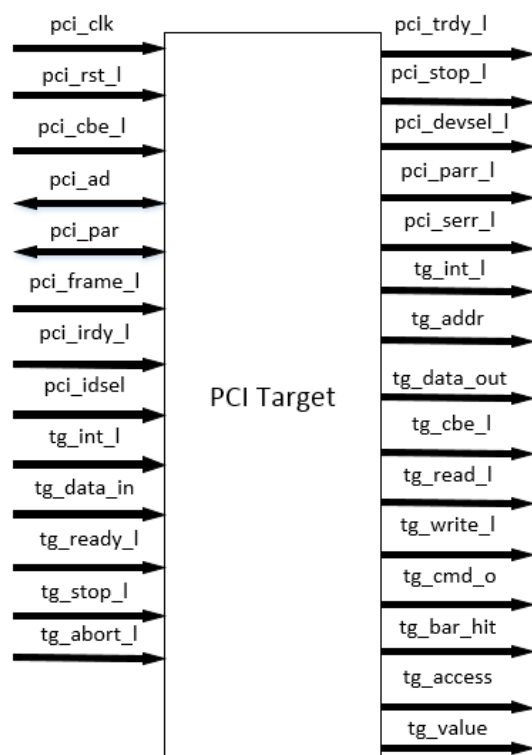
Table 3-10 Max_Lat, Min_Gnt, Interrupt Pin and Interrupt Trunk

Location	Naming	Description
31~24	MAX_LAT	Reserved
23~16	MIN_GNT	Reserved
15~8	Interrupt Pin	The interrupt pin register is used to enable the interrupt pin
7~0	Interrupt Mainline	This is read/write register. The interrupt line register is set by the interrupt handling mechanism to define the interrupt route and it is used to reserve the system interrupt route information

3.5 Ports Description

3.5.1 Ports Diagram

The ports diagram of PCI Target is shown in Figure 3-2.

Figure 3-2 Ports Diagram of PCI Target

3.5.2 Ports Description

The ports description of PCI Target is as shown in Table 3-11.

Table 3-11 Ports Description

Name	I/O	Data Width	Description
PCI interface			
pci_clk	Input	1	System Clock
pci_rst_l	Input	1	Asynchronous reset
pci_ad	Inout	32	Address data multiplexing line
pci_cbe_l	Input	4	Command and byte enable signal multiplexing line
pci_ad	Inout	1	Parity signal
pci_frame_l	Input	1	Frame period signal that indicates the beginning and end of an access.
pci_trdy_l	Output	1	Slave device ready signal When the signal is valid, it indicates that the slave device is ready to transmit data.
pci_irdy_l	Input	1	Master device ready signal When the signal is valid, it indicates that the device initiating the transaction is able to complete a data cycle.
pci_stop_l	Output	1	PCI Target uses this signal to stop the current transaction.
pci_devsel_l	Output	1	Device select signal When the signal is valid, it indicates that the device driving

Name	I/O	Data Width	Description
			it has become the currently accessed slave device.
pci_idsel	Input	1	Initialization device select signal Used as a chip selection signal during parameter configuration read-write transaction.
pci_serr_l	Output	1	System error signal
pci_perr_l	Output	1	Data parity error signal
pci_int_l	Output	1	Interrupt signal output
Backend interface			
tg_addr	Output	32	The signal is used to indicate the address of the transaction
tg_data_out	Output	32	Used as the output when PCI Target write data is transmitted.
tg_data_in	Input	32	Used as the input when PCI Target read data is transmitted.
tg_cbe_l	Output	4	PCI Target byte enable signal
tg_ready_l	Input	1	When the signal is valid, it indicates that the slave device is ready to receive or send data.
tg_write_l	Output	1	When the signal is valid, it indicates that write transaction is currently in progress.
tg_read_l	Output	1	When the signal is valid, it indicates that the read transaction is currently in progress.
tg_stop_l	Input	1	When the signal is valid, it is used to request a stop of transaction on the bus.
tg_abort_l	Input	1	When the signal is valid, it indicates that the transaction on the bus is abandoned
tg_cmd_o	Output	4	This signal is used to lock command information when sending an address during PCI transaction cycle.
tg_bar_hit	Output	0~6	The signal indicates which base is performing bus transaction operation.
tg_access	Output	1	When this signal is valid, it indicates that PCI Target can access the local interface
tg_value	Output	1	When the signal is valid, the data is valid.
tg_int_l	Input	1	When this signal is valid, it indicates that the local interface requires an interrupt.

Note!

*_l means active-low.

3.6 Timing Description

The introduction of waveforms of PCI Target timing is as shown in Table 3-12.

Table 3-12 Description of Waveforms

Symbol	Description
	Drive signal
	Bus data signal or parity signal
	The waveform represents no concern for the signal status here.

3.6.1 Basic Read and Write Timing

PCI Target basic read and write operations refer to reading and writing one data at a time to the I/O address space or memory space. It should be noted that the biggest difference between read and write is that there is no exchange cycle between the address cycle and the data cycle during the write operation. For the specific timing, please see Figure 3-3 and Figure 3-4.

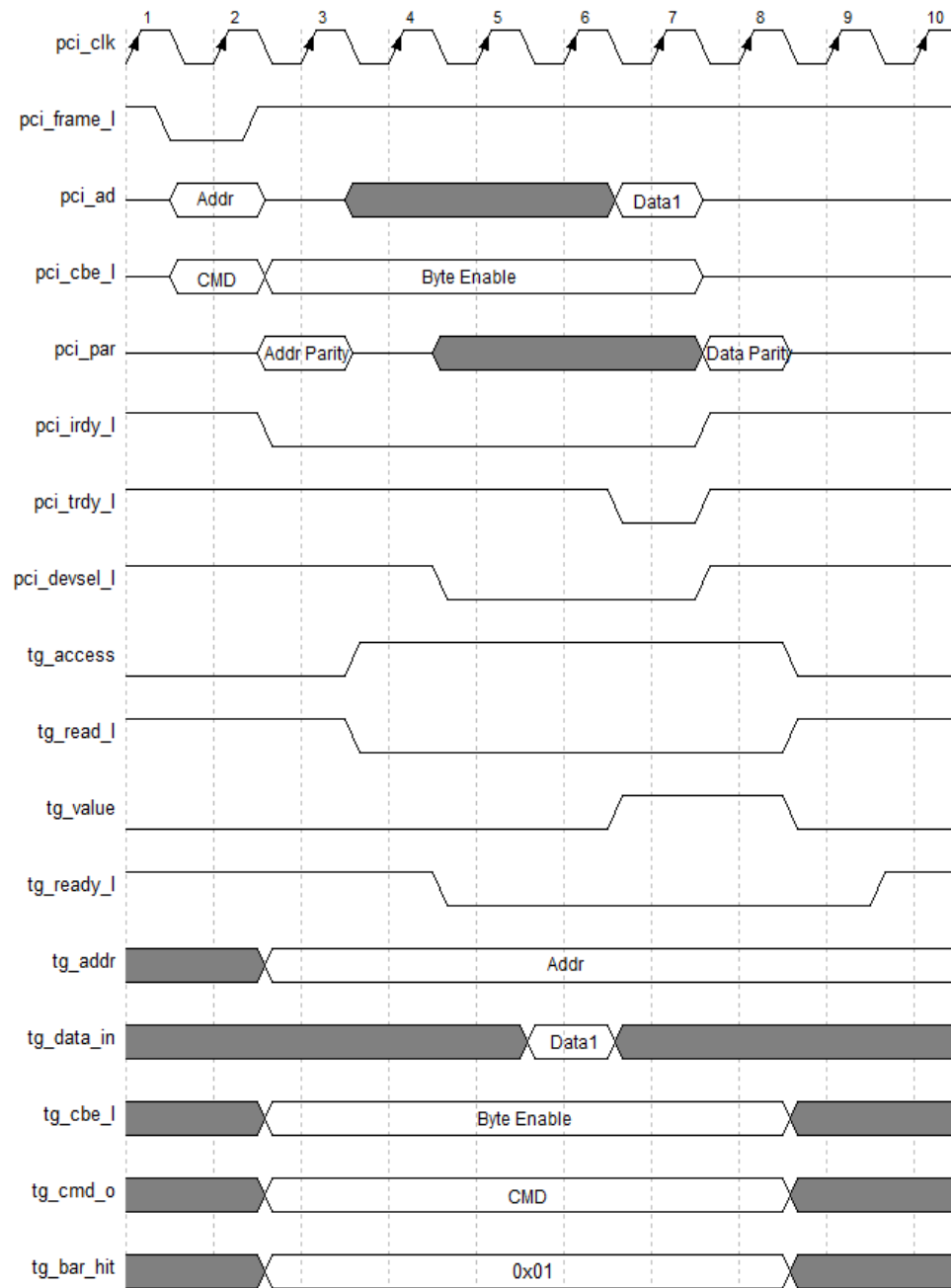
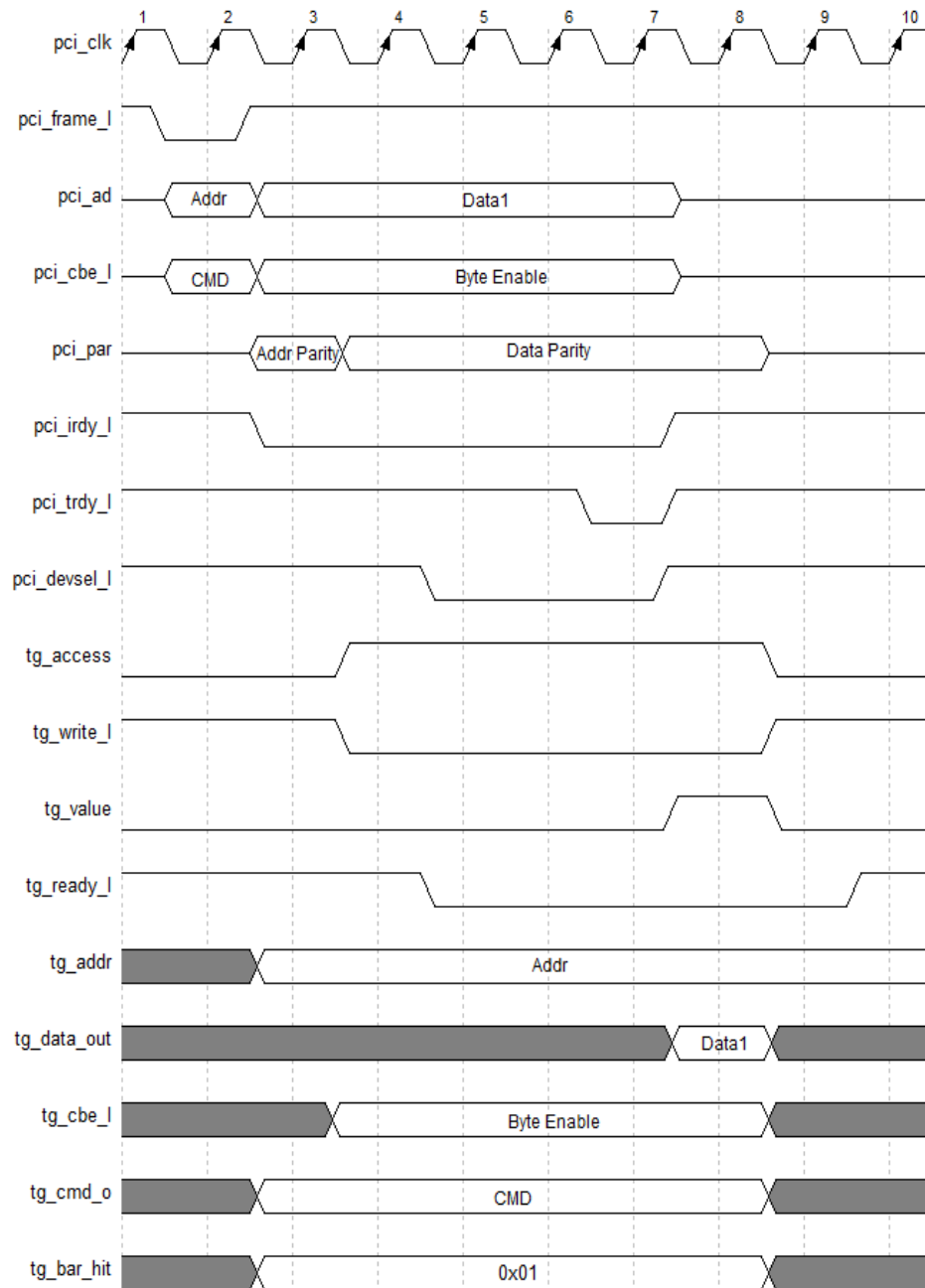
Figure 3-3 Basic Read Transmission

Figure 3-4 Basic Write Transmission

3.6.2 Register Read and Write

According to Table 3-1, when **pci_cbe_l** is equal to 4'b1010 or 4'b1011, it is performing read or write operation, which is to process the data of configuration space. PCI Target only supports 32-bit data transmission configuration. The timing of PCI Target IP configured read and write is as shown in Figure 3-5 and Figure 3-6.

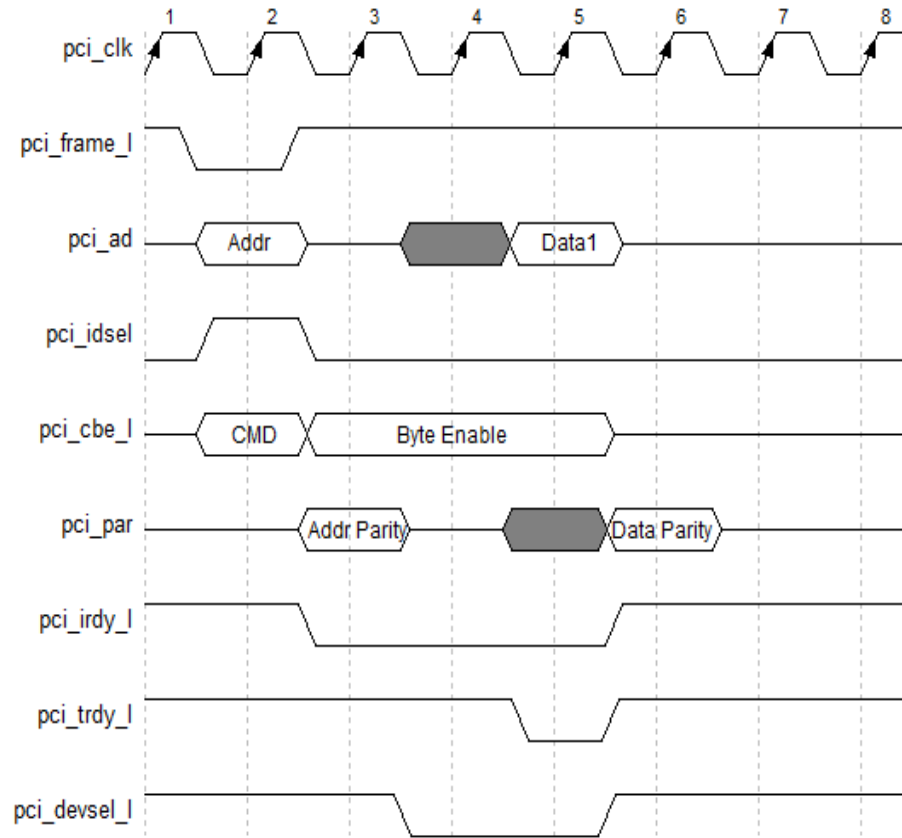
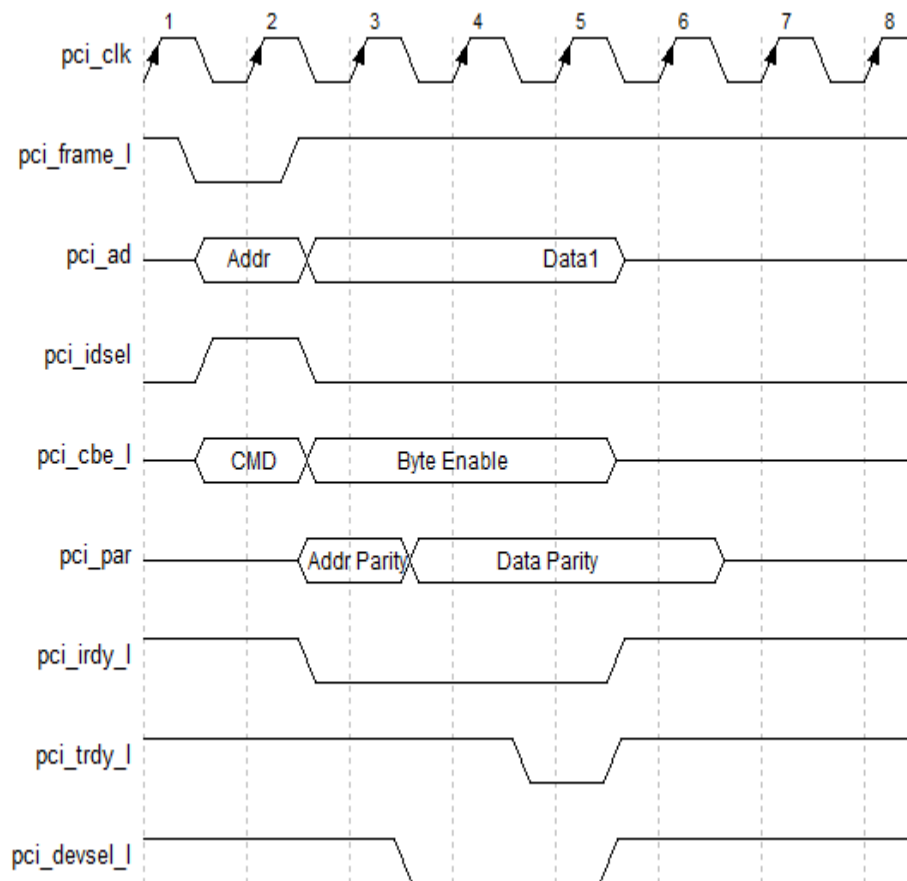
Figure 3-5 Basic Configured Read Transmission

Figure 3-6 Basic Configured Write Transmission

3.6.3 Advanced Target Transactions

In addition to the basic data read write operations described above, there is also PCI Target advanced target transmission. The read/write operation with master waiting cycle is as shown in Figure 3-7 and Figure 3-8. If a waiting cycle is inserted while the master is in PCI Target transmission, the data transmission must be stopped until the master is ready again.

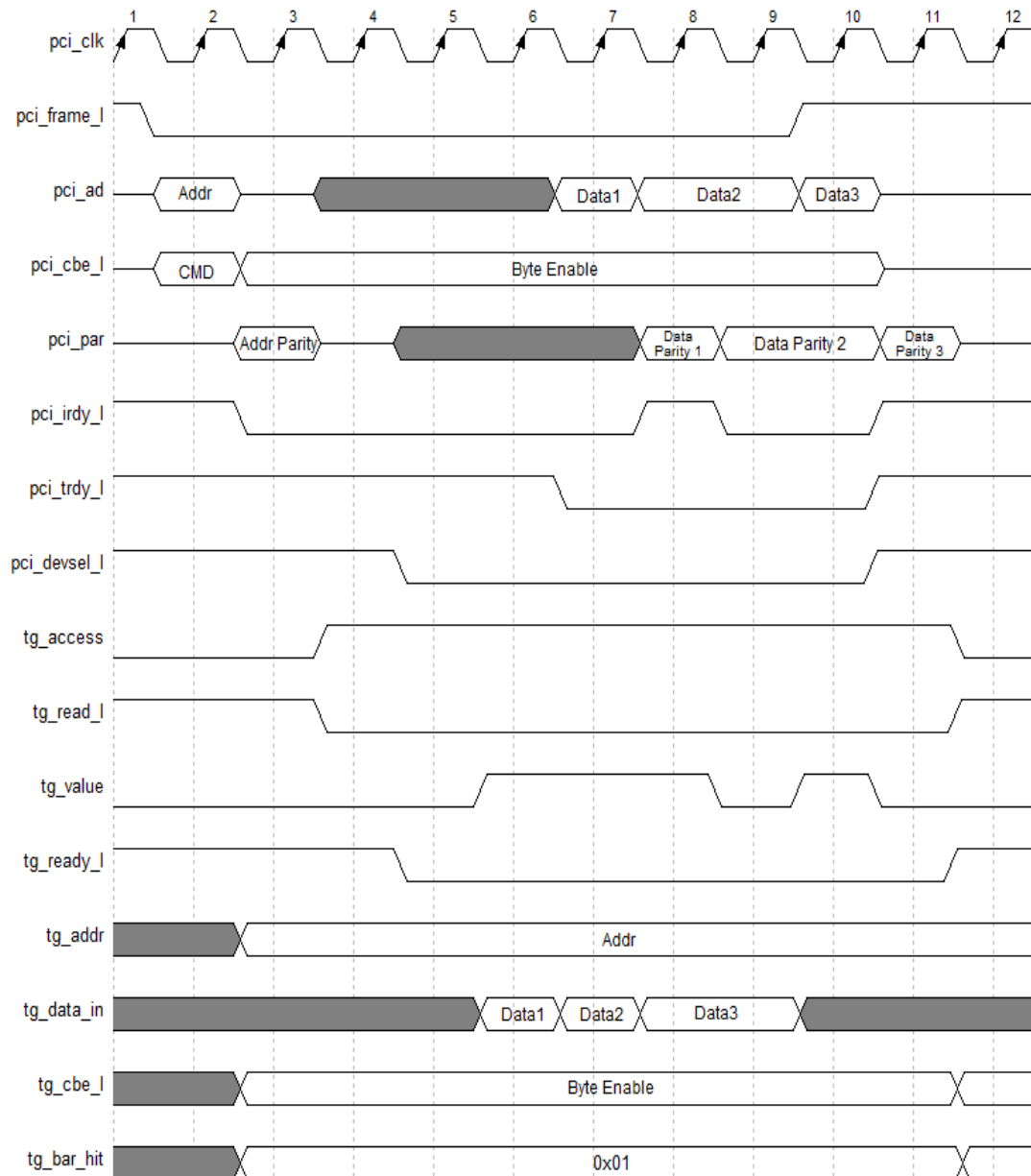
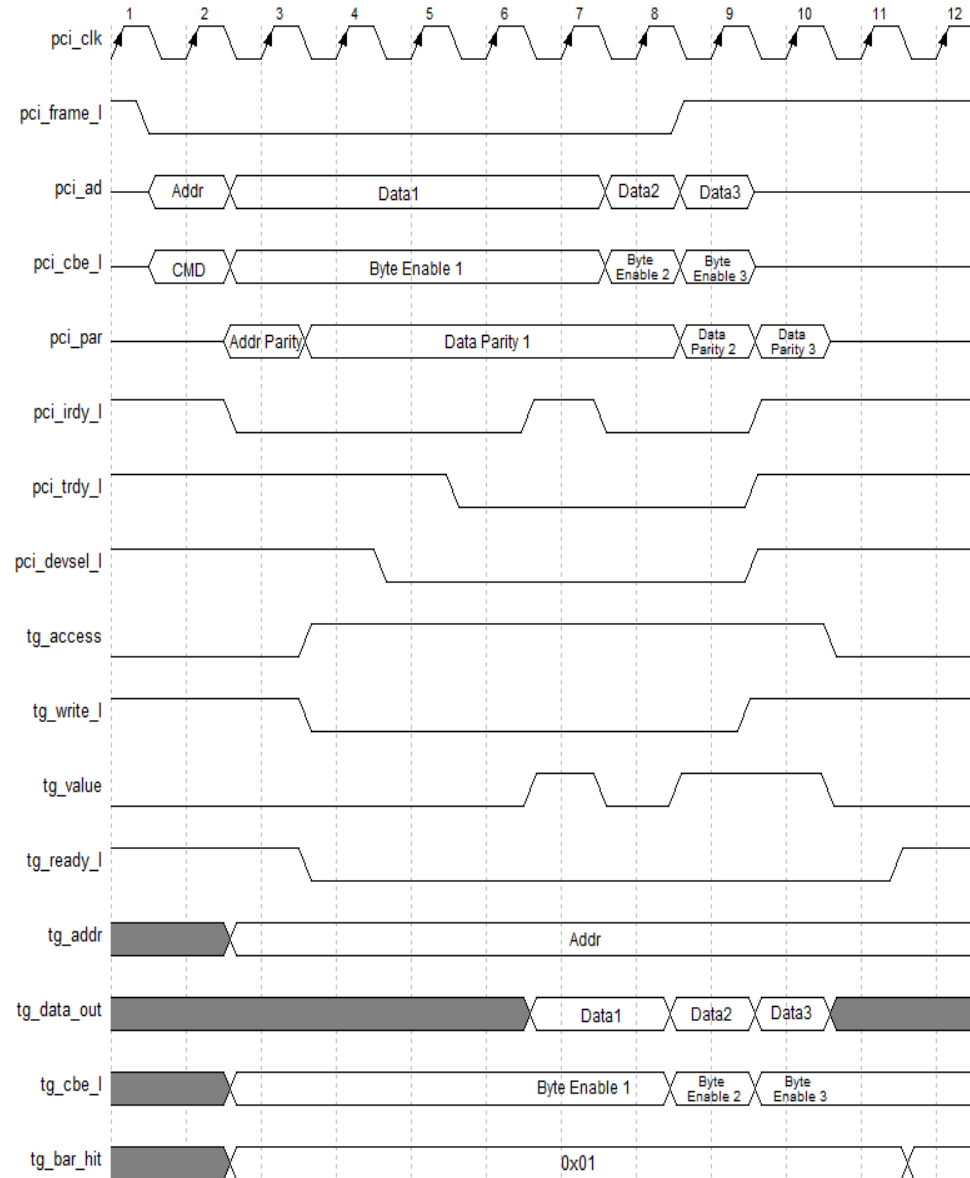
Figure 3-7 Write Transmission with Master Wait Cycle

Figure 3-8 Write Transmission with Master Wait Cycle

The burst read and write timing is as shown in Figure 3-9 and Figure 3-10. It means that multiple data transmissions are required for one read and write. It can be seen that the biggest difference between one data burst read/write operation and read/write operation is that the pci_frame_l signal has a longer effective cycle, which means that there are multiple data to be transmitted.

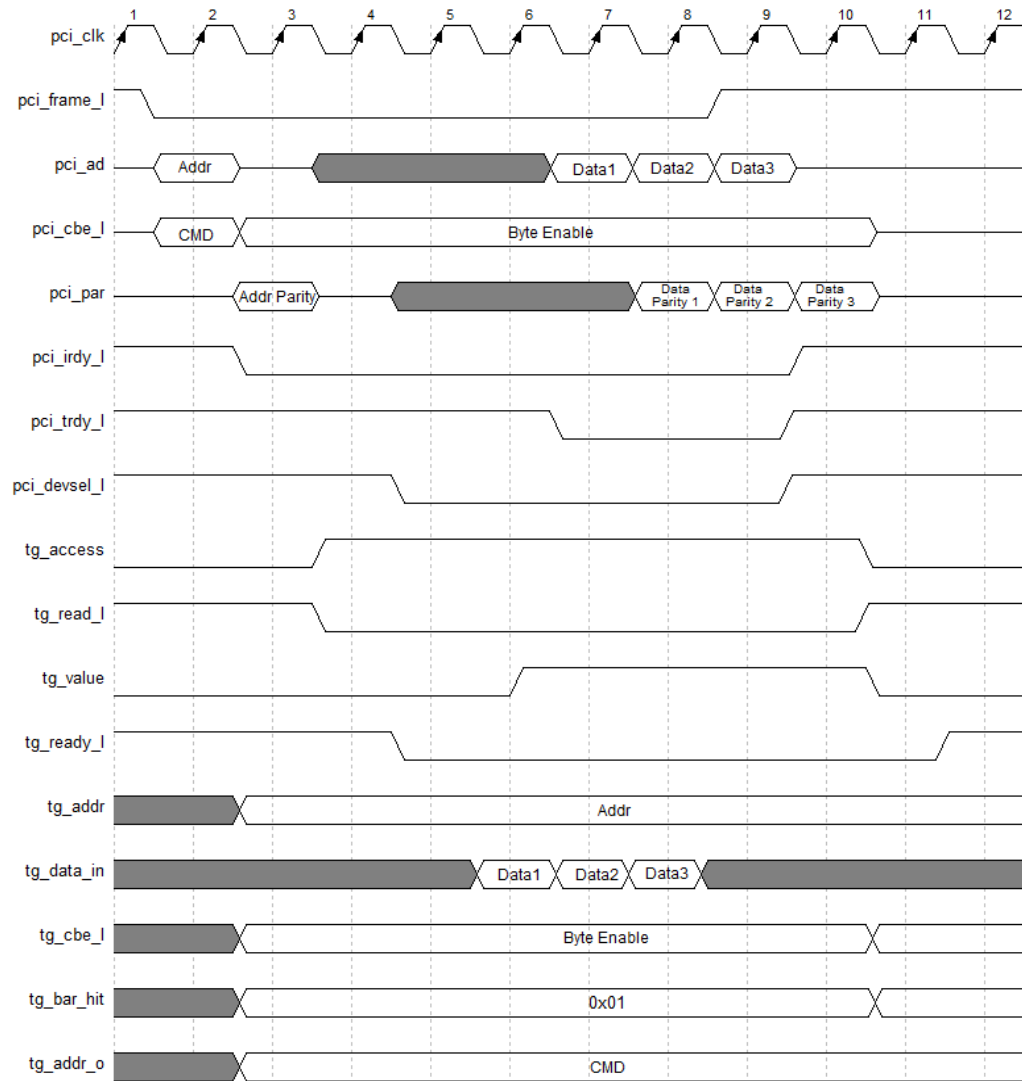
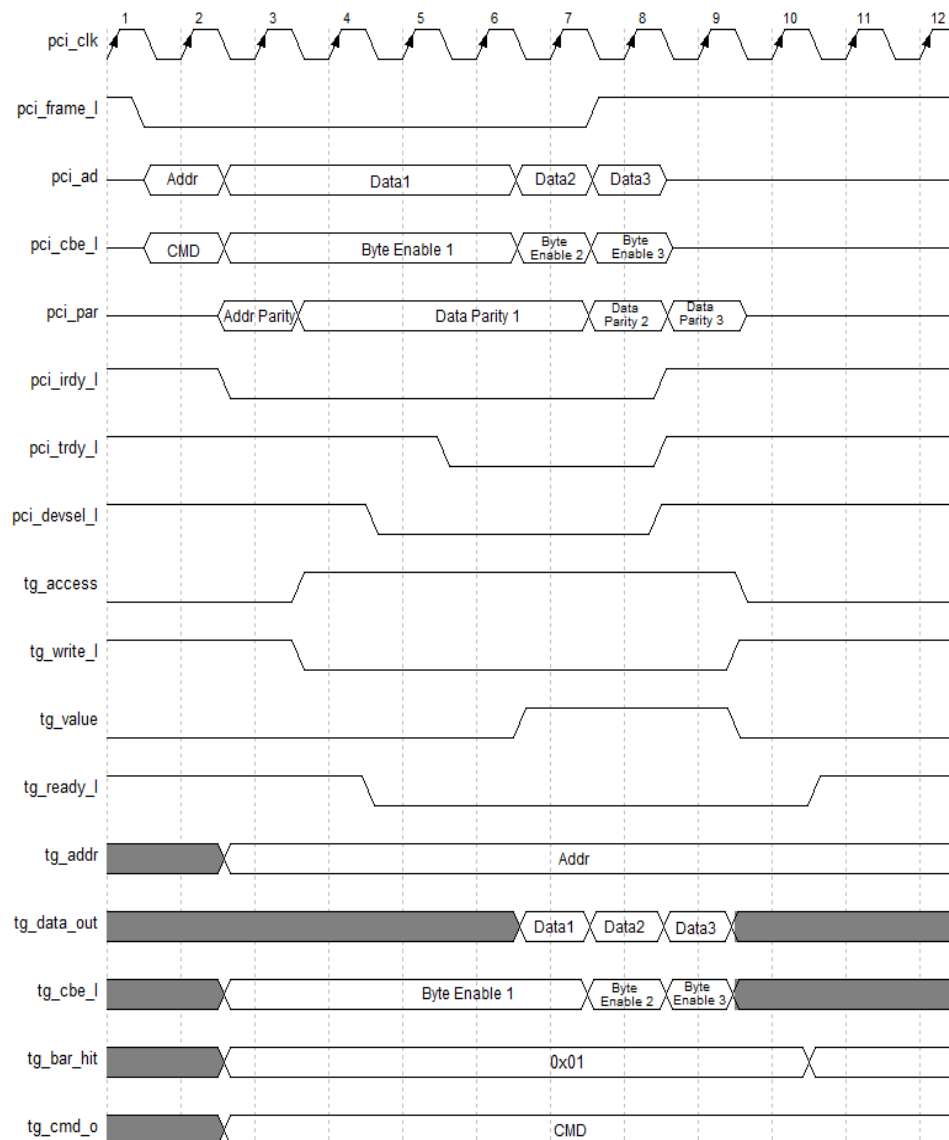
Figure 3-9 Burst Read Transmission

Figure 3-10 Burst Write Transmission

3.6.4 Target Termination

The backend slave device can control PCI transmission of requested information to terminate local interface, and PCI Target should handle each termination type correctly. It is emphasized here that if the slave device wants to terminate a transmission, a `tg_stop_l` signal should be sent from the slave device, and then the PCI Target will send a `pci_stop_l` signal to the master. The `pci_stop_l` signal will remain valid until the `pci_frame_l` signal is revoked.

There are many kinds of termination operations proposed by the slave device, among which the realization of "retry" function is the basic requirement of the protocol, and the rest are optional. Gowin PCI Target IP supports multiple termination operations, as described below.

The timing of the PCI Target Disconnect With Data operation is as shown in Figure 3-11 and Figure 3-12, which can be understood the slave device wants to terminate the current data transaction but retains the last valid data.

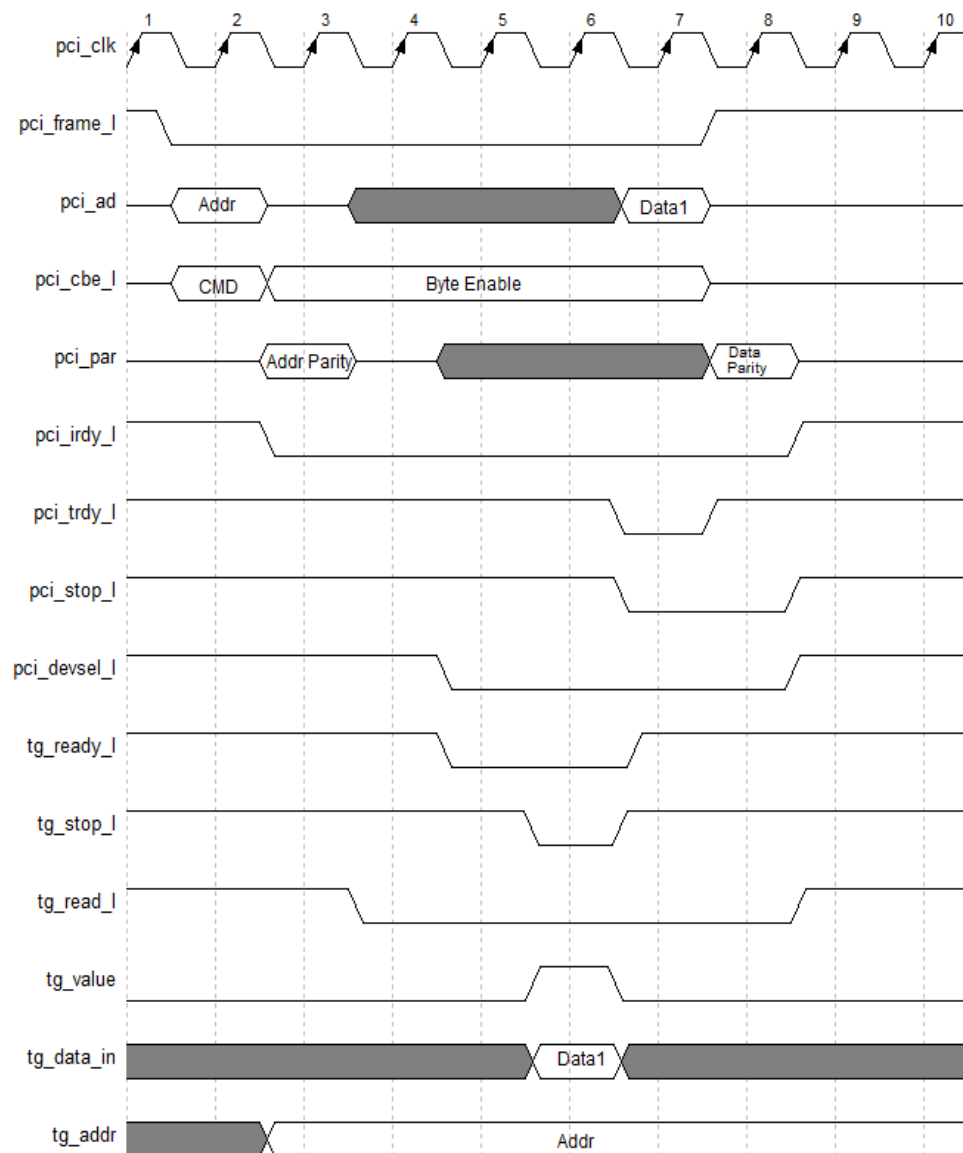
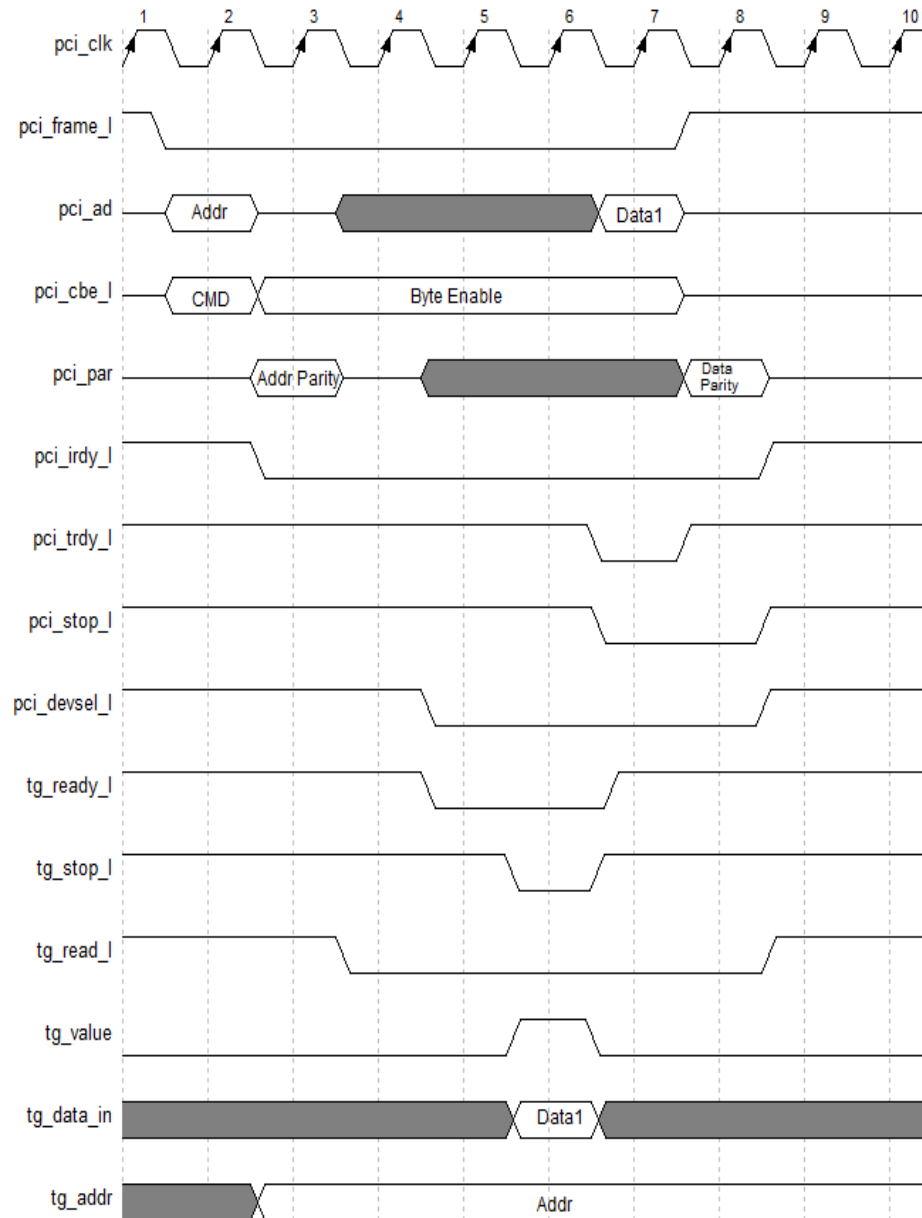
Figure 3-11 Disconnect With Data Read

Figure 3-12 Disconnect With Data Write

The timing of PCI Target "Disconnect Without Data" is as shown in Figure 3-13 and Figure 3-14, which can be understood slave device wants to terminate the current data transmission without retaining any data.

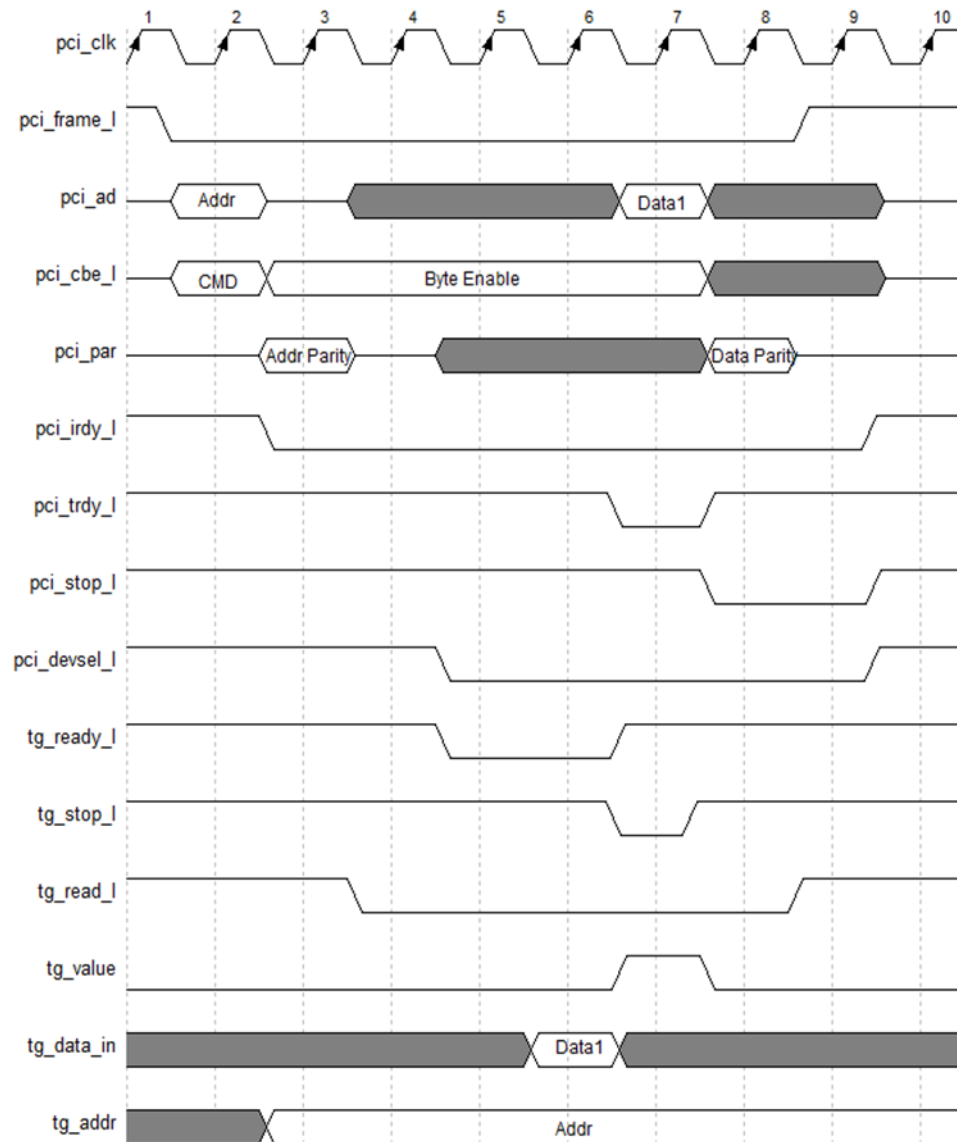
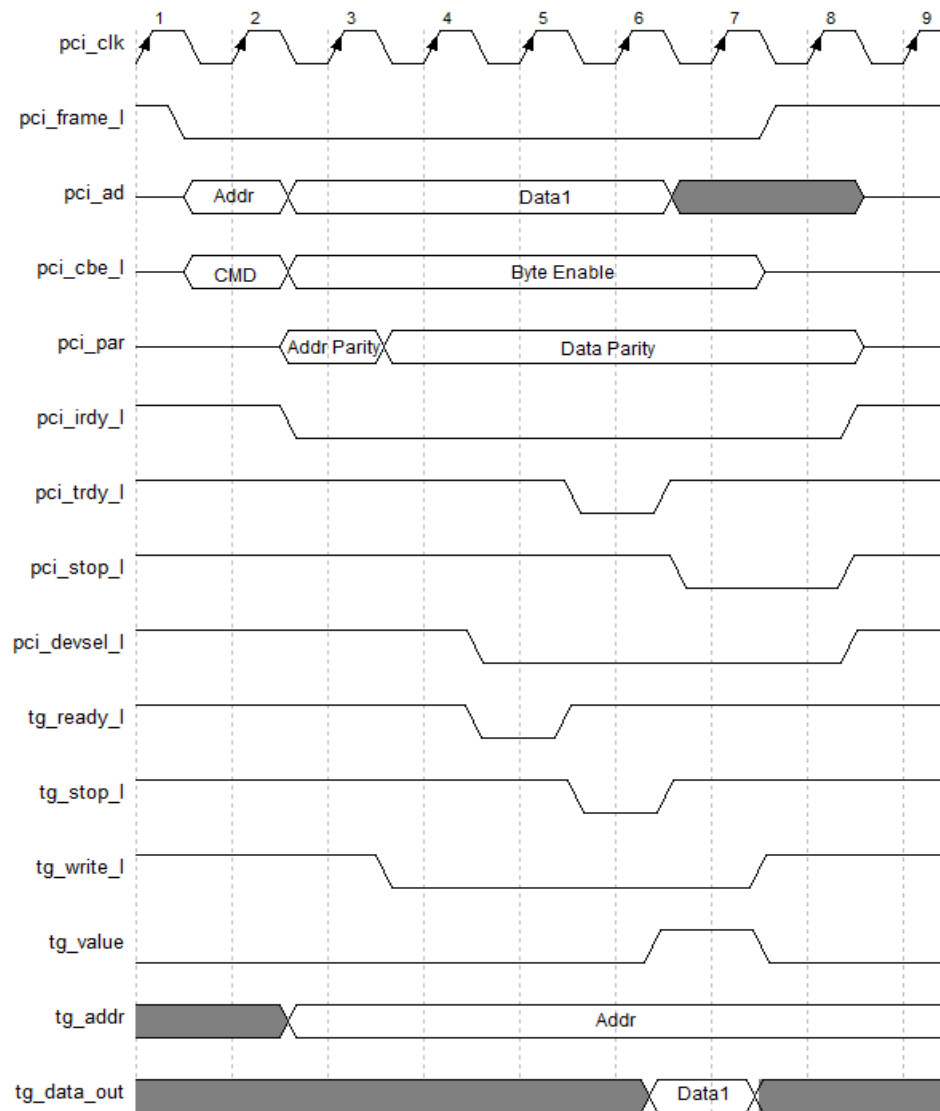
Figure 3-13 Disconnect Without Data Read

Figure 3-14 Disconnect Without Data Write

When the PCI Target does not receive valid `pci_trdy_l` signal and the backend slave device sends `tg_stop_l`, it will do "Retry" operation. In general, this operation may occur because the current slave device is unable to perform normal transmission due to deadlock or some non-PCI resources in a non-idle state or the device in a locked state with mutually exclusive access and so on. In other words, there is no data transmission from the current slave device. The timing of PCI Target Retry Read/Write is as shown in Figure 3-15 and Figure 3-16.

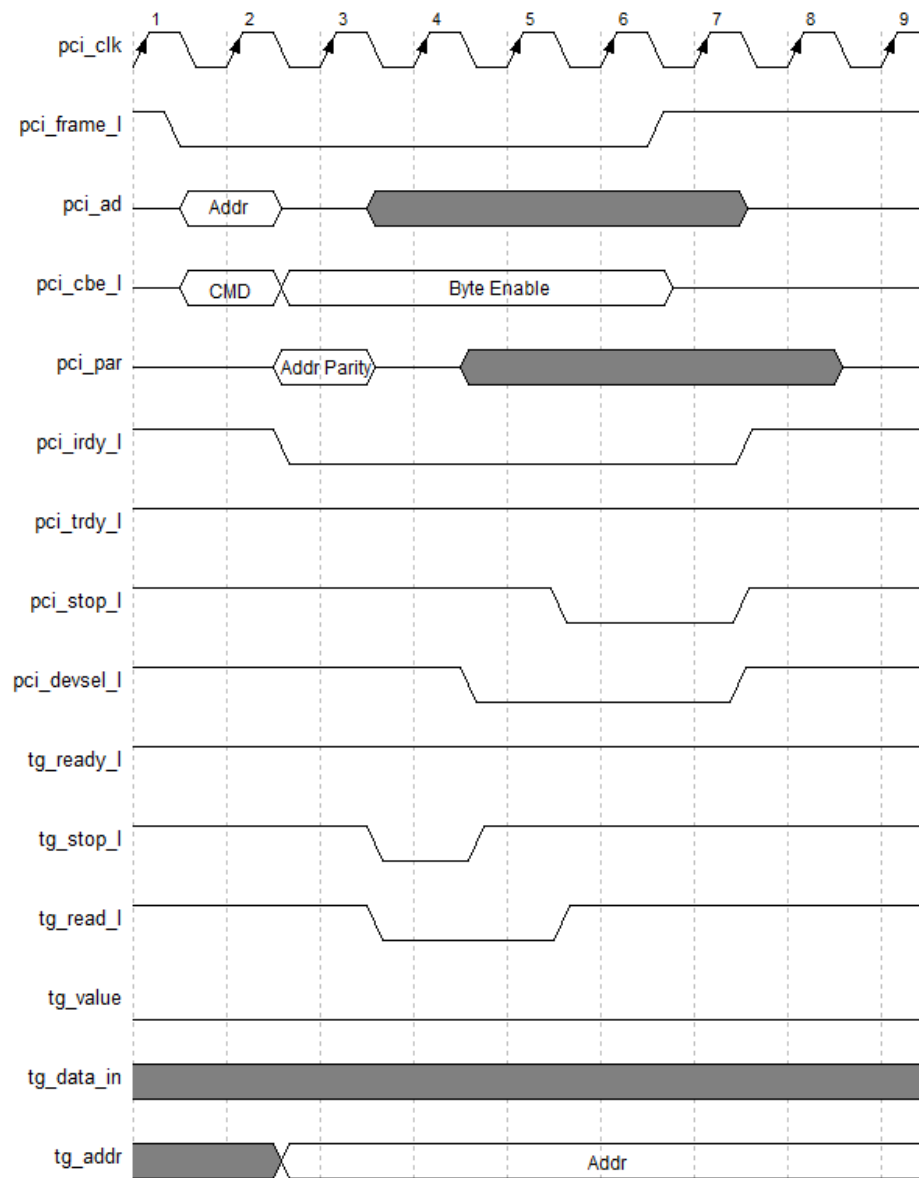
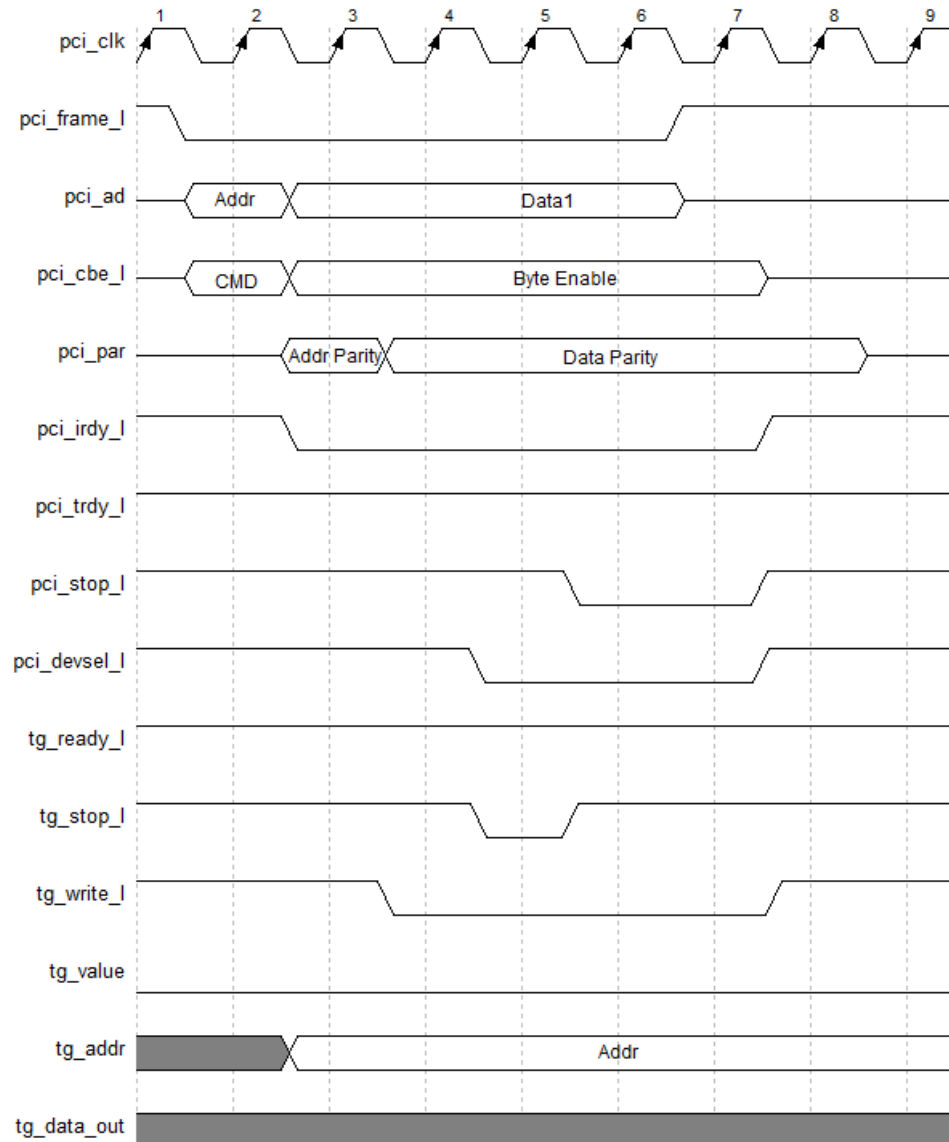
Figure 3-15 Retry Read

Figure 3-16 Retry Write

The **pci_irdy_l** signal has no effect on the transmission when Target abort occurs. The timing of PCI Target Abort Read/Write is as shown in Figure 3-17 and Figure 3-18.

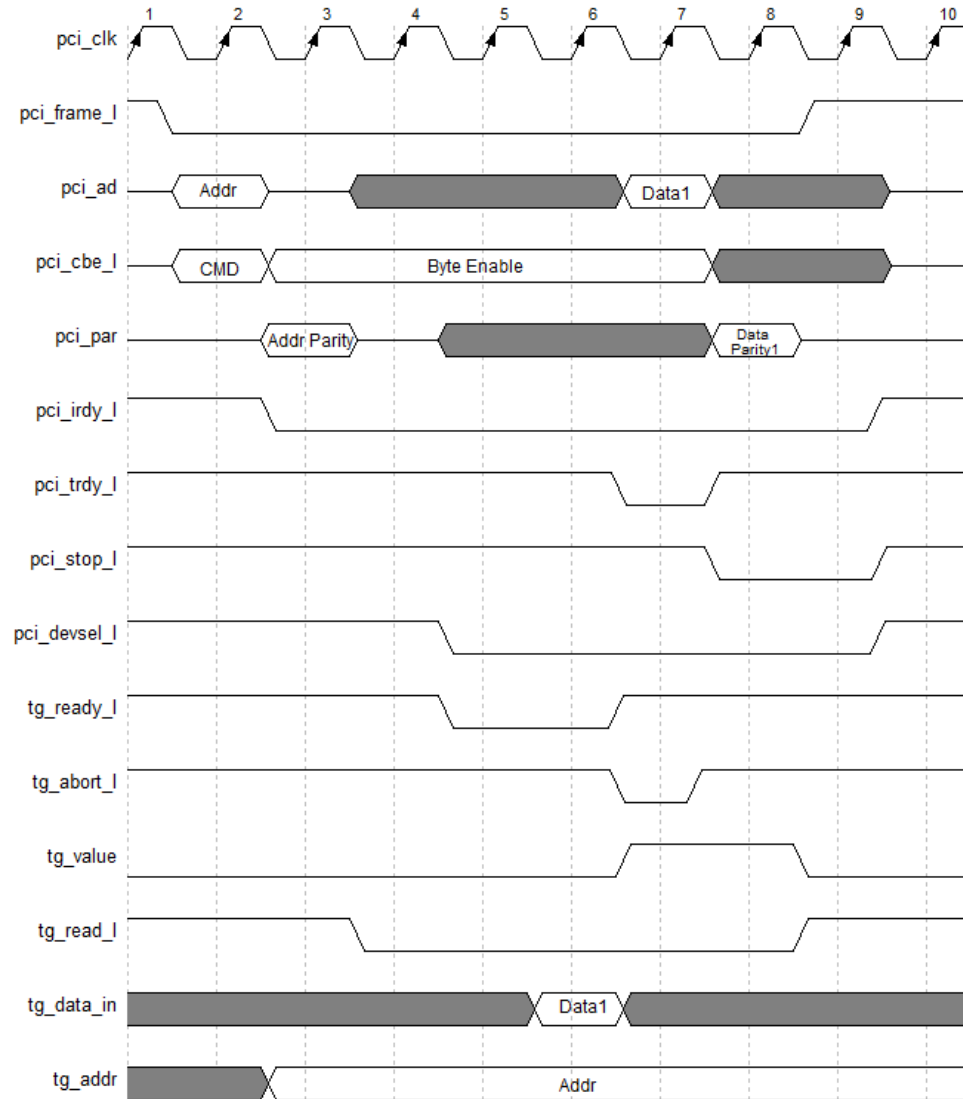
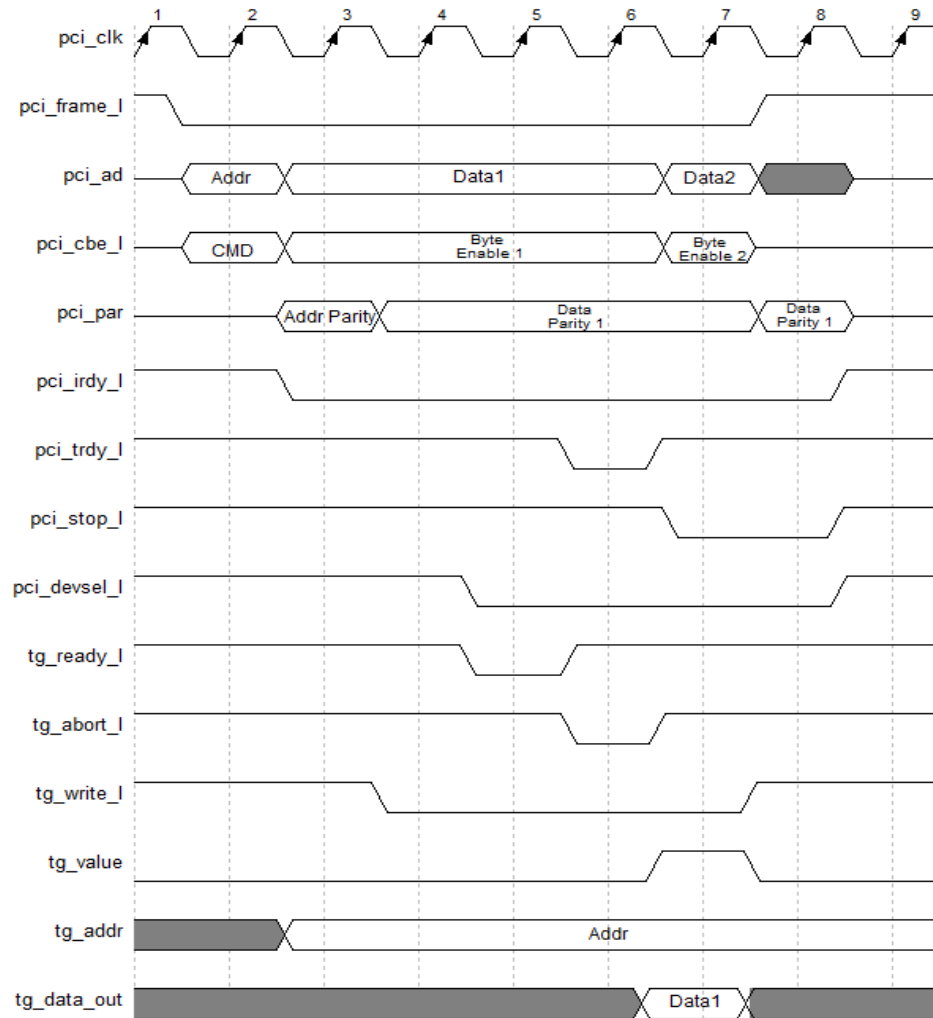
Figure 3-17 Abort Read

Figure 3-18 Abort Write

4 Parameter Configuration

This chapter explains Gowin PCI Target IP parameters configuration interface via IDE GUI.

PCI Target IP configuration interface is as shown in Figure 4-1 and Figure 4-2.

Figure 4-1 PCI Target IP ID Configuration Interface

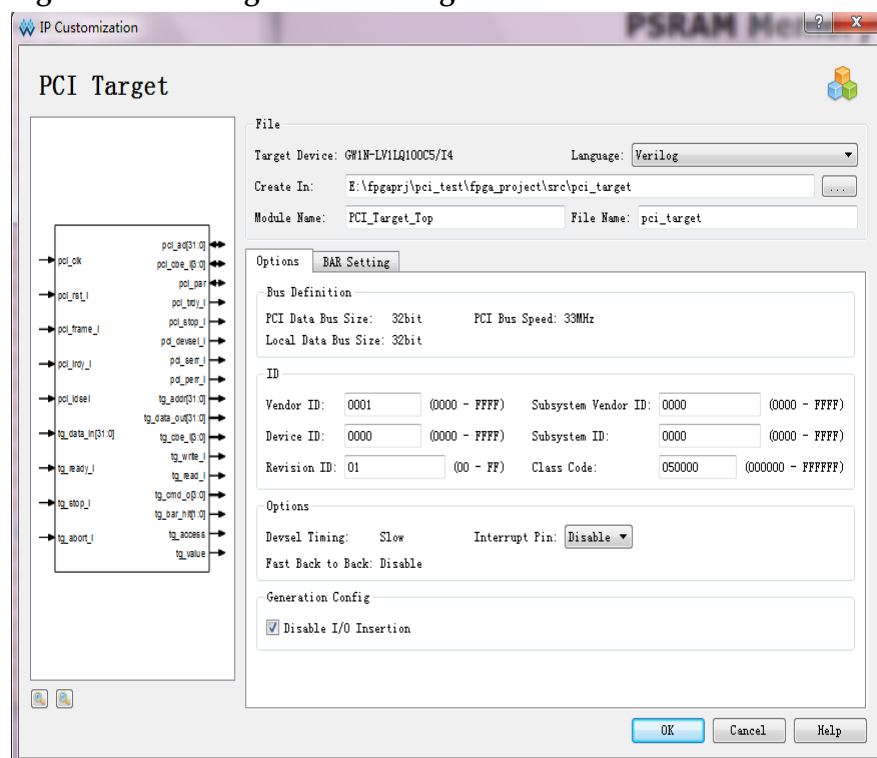
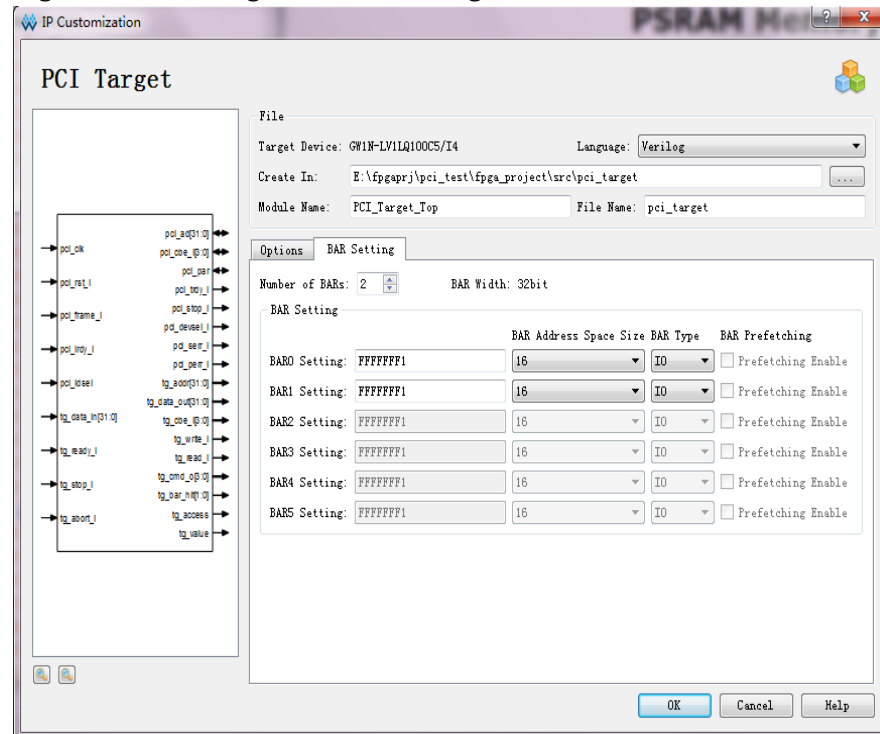


Figure 4-2 PCI Target IP BAR Configuration Interface



The description of parameters in GUI interface is as shown in Table 4-1.

Table 4-1 Parameter Configuration

Parameter	Meaning	Range	Default Value
ID			
Vendor ID[15:0]	Vendor ID	0x0000-0xFFFF	0x0001
Device ID[15:0]	Device ID	0x0000-0xFFFF	0x0000
Subsystem Vendor[15:0]	Subsystem Vendor ID	0x0000-0xFFFF	0x0000
Subsystem ID[15:0]	Subsystem ID	0x0000-0xFFFF	0x0000
Revision ID[7:0]	Revision ID	0x00-0xFF	0x01
Class Code	Class Code	0x000000-0xFF FFFF	0x050000
BARs			
Number of BARs	Number of BARs	0-6	2
BAR0	BAR 0	0x00000000-0xF FFFFFFF	0xFFFFFFFF1
BAR1	BAR 1	0x00000000-0xF FFFFFFF	0xFFFFFFFF1
BAR2	BAR 2	0x00000000-0xF FFFFFFF	0xFFFFFFFF1
BAR3	BAR 3	0x00000000-0xF FFFFFFF	0xFFFFFFFF1

Parameter	Meaning	Range	Default Value
BAR4	BAR 4	0x00000000-0xFFFFFFFF	0xFFFFFFFF1
BAR5	BAR 5	0x00000000-0xFFFFFFFF	0xFFFFFFFF1
BAR0 to BAR5 Configuration Option			
BAR Type	BAR Type	Memory, IO	IO
Address Space Size	Address Space Size	16bytes,32bytes,...,2G	16bytes
Prefetching	Prefetching	Enable, disable	disable

Note!

For more details on register configuration, please see [3.4 Register Configuration](#) section.

