



Gowin I3C DDR eXtension

Release Note

RN524-1.0E, 2018-12-17

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Revision

Date	Revision	Description
2018/12/17	1.0E	Initial version released.

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1 About This Release

This release of I3C DDR eXtension supports IP Core Generator compilation to generate I3C DDR soft core.

The reference design has been configured with specific parameters that can be used for simulation and instantiation of the overall synthesis, placement and routing after user design.

2Overview

Gowin I3C DDR eXtension IP is used in serial communication interfaces and serial sensor interfaces to receive or transmit data. I3C The I3C DDR eXtension provides an I3C bus communication controller with a synchronous SRAM interface.

Table 2-1 Overview of I3C DDR EXtension

I3C DDR eXtension	
IP core application	
Chip supported	GW1N, GW1NR series GW2A, GW2AR series
Delivery document	
Designing documents	Verilog (encrypted)
Reference design	Verilog
TestBench	Verilog
Test design flow	
Integrated software	Synplify_Pro
Application	GowinYunYuan

3Document

The released IP manuals are listed in the table below. You can download the PDF manuals at Gowin website or read online.

Document	Use
Gowin I3C DDR eXtension user guide.pdf	PDF

4IP Support

Because the user design and the highest frequency requirements are different, the reference design does not have associated FPGA-specific location (.cst) and timing constraints (.sdc), and the user can determine it as needed.

For customized IP design and support, please contact the Gowin Sales and Support Hotline

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