Gowin DDR2 Memory Interface IP

Release Note

RN506-1.1E,03/22/2018

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Revision History

Date	Version	Description
08/29/2017	1.0E	Initial version published.
03/22/2018	1.1E	Gowin DDR2 Memory Interface IP is released according to design.

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1 About This Release

This release includes Gowin DDR2 Memory Interface IP reference design and IP Core Generator supports Gowin I3C IP generation.

Gowin DDR2 Memory Interface IP reference design is available at Gowin Website. Take a specific parameter as an example for the reference design, which can be used for simulation and instantiation of the overall synthesis, placement and routing after user design.

2 Overview

Gowin DDR2 Memory Interface IP is a common DDR2 memory interface IP that complies with the JESD79F standard protocol. Gowin DDR2 Memory Interface IP provides the user a generic command interface to connect with the memory chip to access and save. The IP includes the DDR2 Memory Controller (MC) and the corresponding Physical Interface (PHY) design.

Table 2-1 Gowin DDR2 Memory Interace IP

Gowin DDR2 Memory Interface IP	
IP Core Application	
Supported Devices	GW2A-18, GW2AR-18, GW2A-55
Delivered Files	
Design Files	Verilog (encrypted)
Reference Designs	Verilog
TestBench	Verilog
Test and Design Flow	
Integrated Software	Synplify Pro_N-2017.09G-SP1-Beta2
Application Software	GowinYunYuan_V1.8.0Beta1

3 File

The software release file contains Gowin DDR2 Memory Interface IP User Guide, which is listed below:

File	IP Core Generation
Gowin DDR2 Memory Interface IP User Guide.pdf	PDF

4 IP Support

Since the requirements of user design and the highest frequency are different, the reference design does not have associated FPGA specific location (.cst) and timing constraints (.sdc) documents, which the user can determine as required.

For the customized IP design and support, please contact Gowin sales and support line.

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