



# Gowin DDR2 Memory Interface IP User Guide

IPUG506-1.5E, 11/14/2023

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## Revision History

| Date       | Version | Description                                                                                                                                       |
|------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 01/04/2018 | 1.0E    | Initial version published.                                                                                                                        |
| 07/25/2018 | 1.2E    | The port name and port description updated.                                                                                                       |
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| 11/14/2023 | 1.5E    | <ul style="list-style-type: none"><li>● GW5A(S)(T) devices and related descriptions added.</li><li>● Chapter 5 Notes on IP Usage added.</li></ul> |

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# 1 About This Guide

## 1.1 Purpose

Gowin DDR2 Memory Interface IP user guide is designed to help you to quickly learn the features of Gowin DDR2 Memory Interface IP. It includes descriptions of the structure and function of the IP, port, timing specification, configuration & call, reference design, etc. The software screenshots in this manual are based on 1.9.9 Beta-6. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

**Note!**

- When the clock ratio is 1:2, it is applicable to GW2A, GW2AN, GW2AR, and GW2ANR devices.
- When the clock ratio is 1:4, it is applicable to GW5A, GW5AR, GW5AS, GW5AST, and GW5AT devices.
- If there is no specific explanation, it means that the using method for both 1:2 and 1:4 clock ratios is the same. Any differences will be described in their respective sections.

## 1.2 Related Documents

The latest user guides are available on the Gowin website. Refer to the related documents at [www.gowinsemi.com](http://www.gowinsemi.com):

- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS971, GW2AN-18X & 9X Data Sheet](#)
- [DS976, GW2AN-55 Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS1103, GW5A series of FPGA Products Data Sheet](#)
- [DS1104, GW5AST series of FPGA Products Data Sheet](#)
- [DS1108, GW5AR series of FPGA Products Data Sheet](#)
- [DS1105, GW5AS series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

## 1.3 Abbreviations and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1.

**Table 1-1 Abbreviations and Terminology**

| Abbreviations and Terminology | Full Name/Meaning        |
|-------------------------------|--------------------------|
| ECC                           | Error Correcting Code    |
| FIFO                          | First Input First Output |
| GSR                           | Global System Reset      |
| IP                            | Intellectual Property    |
| LUT                           | Look-up Table            |
| RAM                           | Random Access Memory     |

## 1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: [www.gowinsemi.com](http://www.gowinsemi.com)

E-mail: [support@gowinsemi.com](mailto:support@gowinsemi.com)

# 2 Overview

Gowin DDR2 Memory Interface IP is a universal DDR2 memory interface IP that conforms to the JESD79-2F standard protocol. This IP includes a DDR2 Memory Controller (MC) and its corresponding Physical Interface (PHY) design. Gowin DDR2 Memory Interface IP provides users with a generic command interface, enabling interconnection with memory chips to access and save data.

**Table 2-1 Gowin DDR2 Memory Interface IP**

| Gowin DDR2 Memory Interface IP |                                         |
|--------------------------------|-----------------------------------------|
| Logic Resource                 | See Table 3-1.                          |
| Delivered Doc.                 |                                         |
| Design Files                   | Verilog (encrypted)                     |
| Reference Designs              | Verilog                                 |
| TestBench                      | Verilog                                 |
| Test and Design Flow           |                                         |
| Integrated Software            | GowinSynthesis                          |
| Application Software           | Gowin Software (V1.9.9Beta-6 and above) |

**Note!**

For the devices supported, you can click [here](#) to get the information.

# 3 Features and Performance

## 3.1 Features

- Supports GW2A-18, GW2AR-18, GW2A-55, GW5AST-138, and GW5A-25 FPGA devices
- Interfaces to the industrial standard DDR2 SDRAM devices and modules that are compatible with the JESD79-2F specification
- For GW2A-18, GW2AR-18, and GW2A-55, the clock ratio is 1:2; for GW5AST-138 and GW5A-25, the clock ratio is 1:4
- Supports memory data path width of 8, 16, 24, 32, 40, 48, 56, 64, and 72 bits.
- Supports the single-row RDIMM UDIMM, and SODIMM memory modules
- Supports memory chips with three data width options: x4, x8, and x16.
- Programs 4 or 8 burst lengths
- Supports ECC
- Configurable CL
- Configurable AL
- Configurable  $t_{FAW}$
- Configurable  $t_{RAS}$
- Configurable  $t_{RCD}$
- Configurable  $t_{RFC}$
- Configurable  $t_{RRD}$
- Configurable  $t_{RTP}$
- Configurable  $t_{WTR}$
- Supports the on-chip dynamic terminal ODT
- Supports automatic refreshing and user startup refreshing, the interval of automatically refreshing configurable

## 3.2 Working Frequency and Bandwidth Efficiency

Gowin DDR2 Memory Interface IP supports the following DDR2 SDRAM data rates:

- 533 Mbps in 1:2 clock ratio mode
- 533 Mbps and 800 Mbps in 1:4 clock ratio mode

Gowin DDR2 Memory Interface IP bandwidth efficiency statistics are as follows:

- In clock ratio 1:2 mode, the burst length is 4 and the bandwidth efficiency is 50%
- In 1:2 clock ratio mode, the burst length is 8 and the bandwidth efficiency is 90%
- In 1: 4 clock ratio mode, bandwidth efficiency is 90%

## 3.3 Resource Utilization

Gowin DDR2 Memory Interface IP employs the Verilog language, which is used in the GW2A-18, GW2AR-18, GW2A-55 GW5AST-138, and GW5A-25FPGA devices. Table 3-1 presents an overview of the resource utilization. For other applications, please see the later release information.

**Table 3-1 Resource Utilization**

| DQ_WIDTH | LUTs | REGs | I/Os | f <sub>MAX</sub> (MHz) | Device Series      | Speed Level    |
|----------|------|------|------|------------------------|--------------------|----------------|
| 8(x8)    | 1061 | 1009 | 151  | 266 MHz<br>(533 Mbps)  | GW2A-55<br>GW2A-18 | -6<br>-7<br>-8 |
| 16(x8)   | 1312 | 1365 | 231  |                        |                    |                |
| 24(x8)   | 1557 | 1721 | 311  |                        |                    |                |
| 32(x8)   | 1639 | 2077 | 391  |                        |                    |                |
| 40(x8)   | 1845 | 2433 | 471  |                        |                    |                |
| 48(x8)   | 2060 | 2789 | 551  |                        |                    |                |
| 56(x8)   | 2271 | 3145 | 631  |                        |                    |                |
| 64(x8)   | 2483 | 3501 | 711  |                        |                    |                |
| 72(x8)   | 2694 | 3857 | 791  |                        |                    |                |

**Note!**

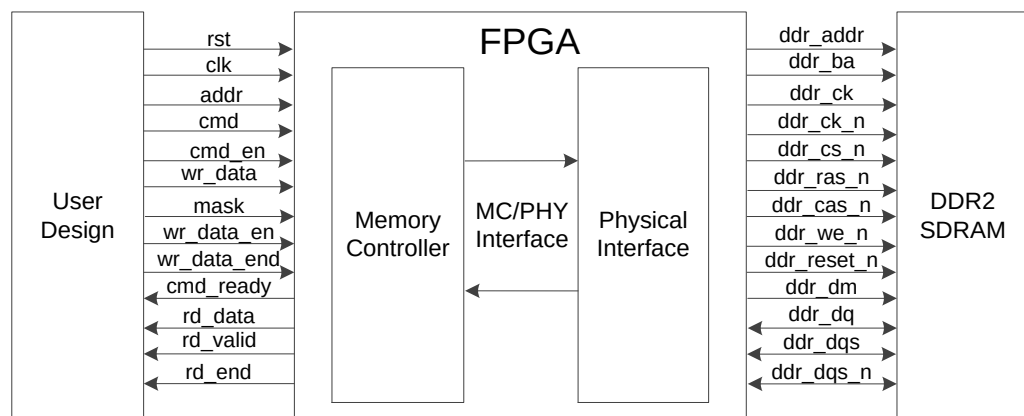
In Table 3-1, Gowin DDR2 Memory Interface is configured with a user address width of 27 bits, and DRAM width of x8.

# 4 Functional Description

## 4.1 Structure

Gowin DDR2 Memory Interface IP consists of a memory controller, physical interface, and other modules. Its basic structure is as shown in Figure 4-1. The user design in Figure 4-1 is the user design connected to the external DDR2 SDRAM chip in FPGA.

Figure 4-1 Structure of Gowin Memory Interface IP



## 4.2 Memory Controller

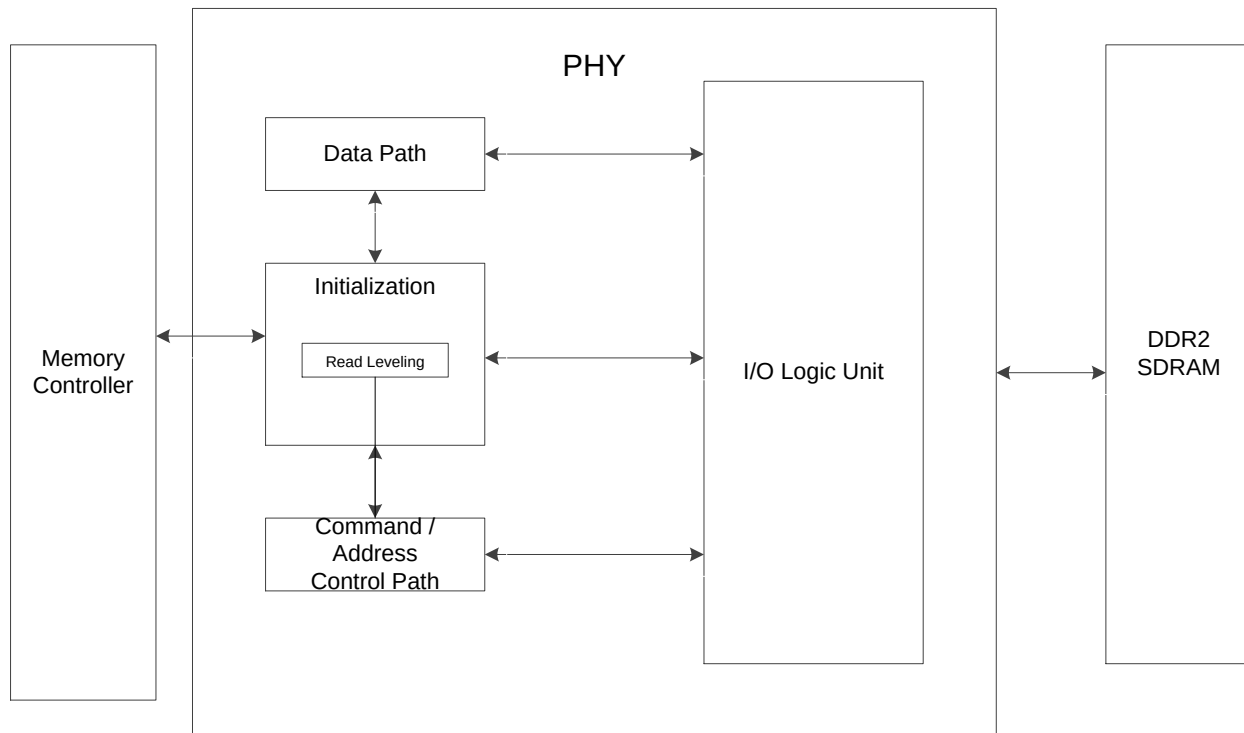
Memory Controller belongs to the MC layer and implements protocol layer functions. The internal state machines control BANK, ROW, COL, and refresh operations. Memory Controller receives user-side read/write commands and stores them internally in a FIFO logic; then these read and write commands are transformed into interface timing recognizable by the PHY side and input them to the PHY side.

## 4.3 PHY

The PHY provides the physical layer definition and interface between the MC and the external DDR2 SDRAM, receives commands from the MC memory controller, and provides the DDR2 SDRAM chip with interface timing.

The basic structure of PHY includes four modules: Initialization module, data path, command address control path, and I/O logic module, as shown in Figure 4-2.

Figure 4-2 Basic Structure of DDR2 PHY



### 4.3.1 Initialization Unit

The initialization module mainly completes the initialization and read calibration of DDR2 SDRAM after power on. After completing all initialization and read calibration, the signal "init\_calib\_complete" will change from low to high, indicating that the whole initialization is completed.

**Note!**

Read/write operations are not allowed until the init\_calib\_complete signal is pulled high.

**Power-on Initialization**

According to the JESD79-2F protocol standard, there is a need to initialize the DDR2 SDRAM (chip or DIMM) after power on. This includes the reset, clock enable, mode register configuration, and ZQ calibration.

### 4.3.2 Data Path Unit

The data path includes writing data and reading data.

### 4.3.3 Control Path Unit

The command/address control path is a unidirectional path that receives the command and address signals sent by the MC and works with the data path to process the write and read data delay parameters and sends the commands to the I/O logic module.

### 4.3.4 I/O Logical Unit

The I/O logic module mainly performs clock domain conversion on the data, command, and address signals passed through the data path and the command/address path.

## 4.4 Major Functions

The functions of the Memory Interface IP are as follows:

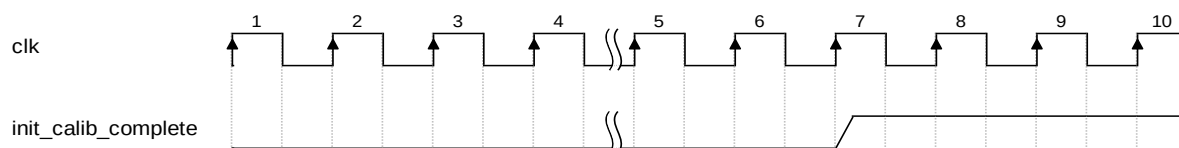
- Initialize DDR2 SDRAM
- Send the addresses and commands
- Write data
- Read data
- Refresh

### 4.4.1 Initialization

DDR2 SDRAM must be calibrated to perform normal write and read operations. Therefore, the PHY will initiate calibration operations on the DDR2 SDRAM after power-on, and once the initialization is complete, it returns the initialization completion flag `init_calib_complete`.

After the initialization is completed, the operation completion signal is returned to the user, as shown in Figure 4-3.

**Figure 4-3 Initialization Completed Signal Timing Diagram**



### 4.4.2 Send Addresses and Commands

#### Address

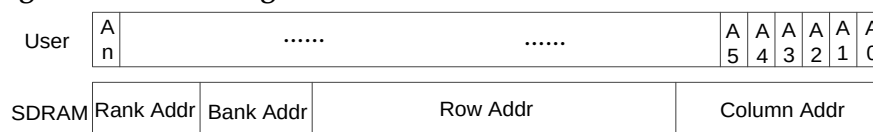
`addr` is the user-side address bus that is written to the controller along with `cmd`. `addr` is valid when `cmd_en` is valid.

- `addr`: address data port

In the application, there is a certain mapping relationship between the address bus of the user interface and the Rank, Bank, Row, and Column of the physical memory. In this design, the addresses are sequentially

arranged in the order of Rank-Bank-Row-Column, and the addressing scheme is shown in Figure 4-4. Users should pay attention to the order of addresses provided in the application.

**Figure 4-4 Addressing Scheme in Rank-Bank-Row-Column Order**



## Command

Users can write commands to the IP via cmd and cmd\_en, and the controller initiates read/write transactions to the DDR2 chip according to the order of the write commands.

- cmd: command data port
- cmd\_en: address and command enable signal, active-high

The meaning of cmd is shown in Table 4-1.

**Table 4-1 cmd**

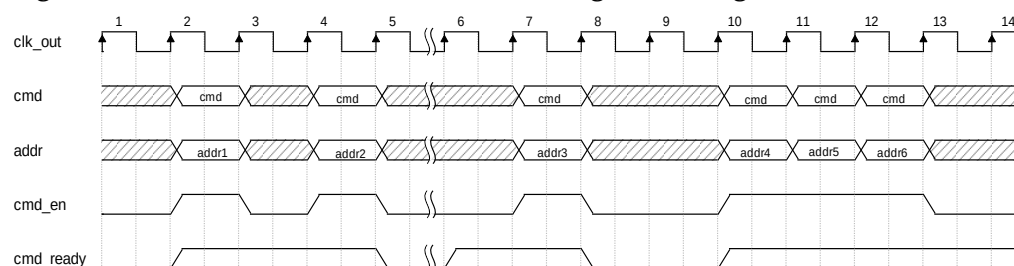
| Command | cmd[2:0] |
|---------|----------|
| Read    | 3'b001   |
| Write   | 3'b000   |

## Address and Command Timing

On the user interface side, the timing between command, address and enable signals is shown in Figure 4-5. cmd\_ready is high, indicating that the MC can receive commands and the commands can be stored in the MC FIFO; if cmd\_ready is low, it will be impossible for the MC to receive commands at this time.

When cmd\_en and cmd\_ready both are 1, the cmd and addr will be written to the IP; addr are independent of each other, that is, addr1 and addr2 do not have any relationship, it does not have to be neighboring addresses.

**Figure 4-5 Command, Address, and Enable Signal Timing**

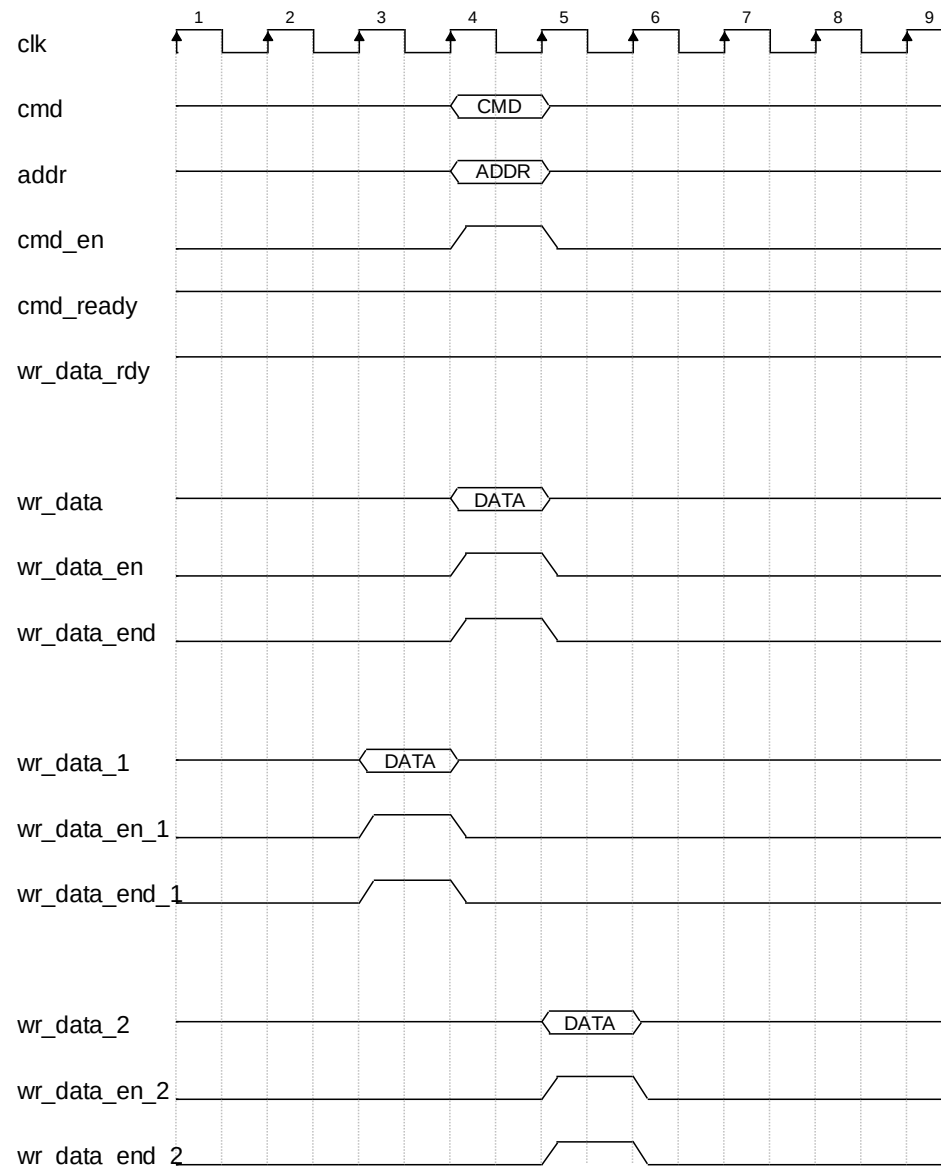


### 4.4.3 Position Relationship between Command and Write Data

The position relationship between cmd and data shown in Figure 4-6.

- Write data is sent at the same time as the write command
- Write data is sent before the corresponding write command
- Write data is sent after the corresponding write command, but delay cycles for write data cannot be 2 cycles.

Figure 4-6 Position Relationship between cmd and Data



### 4.4.4 Write Data

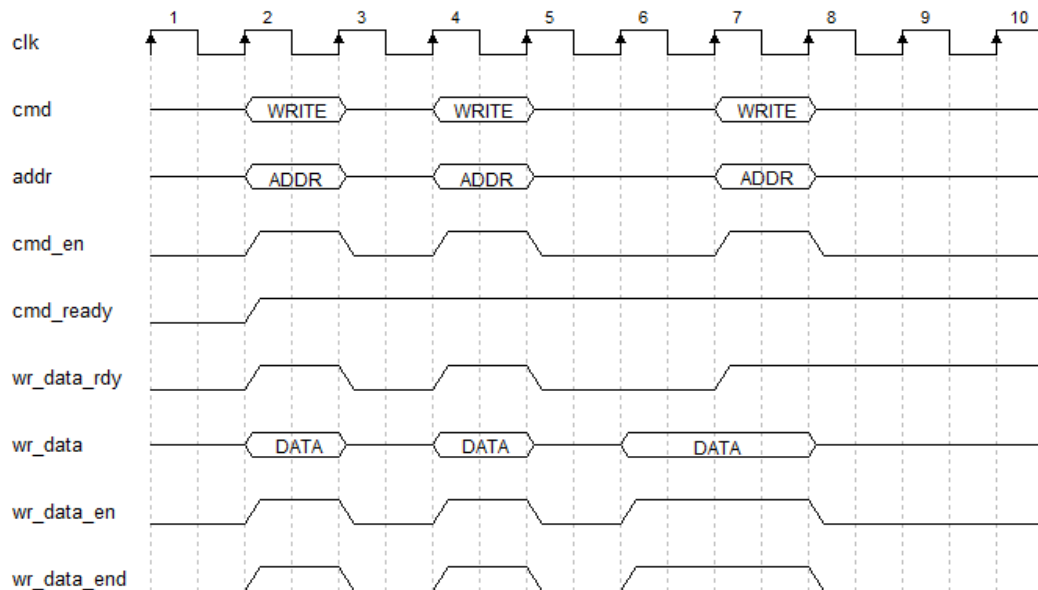
You can send write data to Gowin DDR2 Memory Interface IP through wr\_data, wr\_data\_wren, and wr\_data\_end. And the write data will be processed and sent to the DDR2 SDRAM.

#### Write Data in 1:2 Clock Ratio

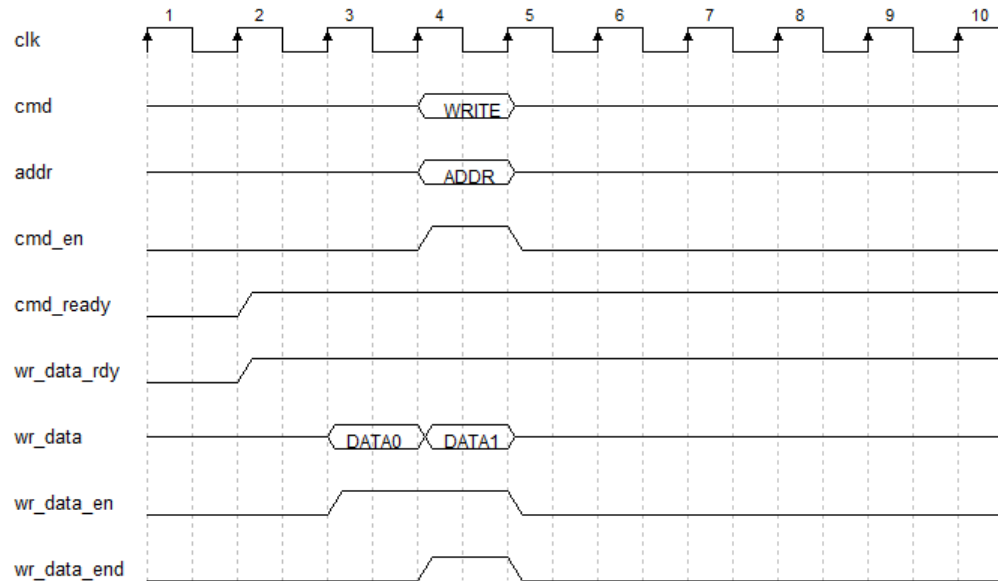
- wr\_data is a write data port

- `wr_data_en` is a write data enable port, active-high
- `wr_data_end` indicates the last cycle to be occupied by this set of data written under the current burst length
- In the write data channel, when `wr_data_rdy` is high, it indicates that the MC is ready to receive write data
- If `wr_data_rdy` is low, and the user sends write data, the signals such as `wr_data`, `wr_data_en` and `wr_data_end` should be maintained until `wr_data_rdy` is high, as shown in Figure 4-7.

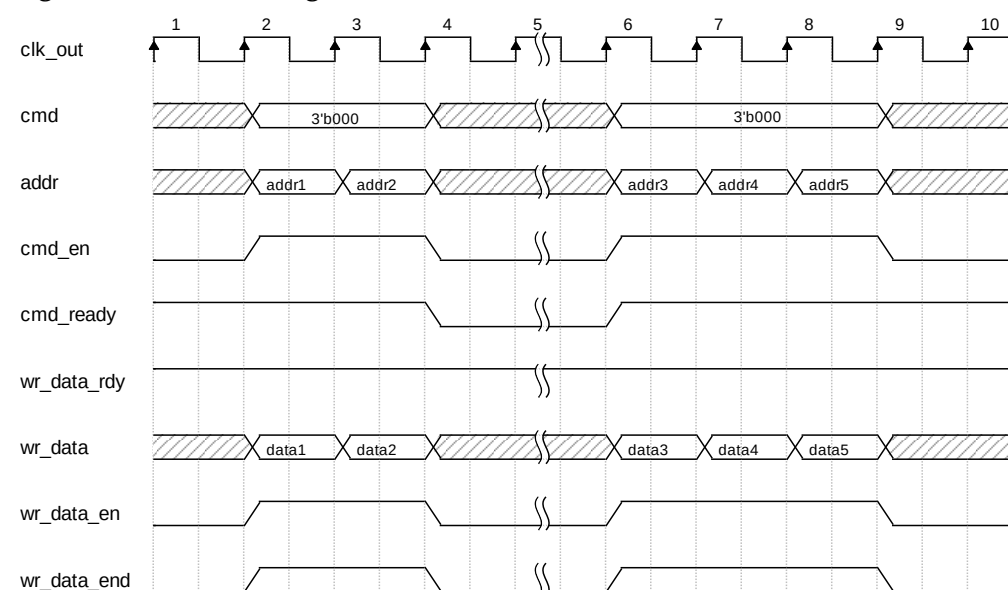
**Figure 4-7 Write Timing in 1:2 Clock Ratio**



When the clock ratio for MC and PHY is 1:2, the write data occupies two CLK cycles if the user configures a BL8 burst length, as shown in Figure 4-8. The `wr_data_end` changes to a high level during the second cycle of writing data to indicate the end of the write data.

**Figure 4-8 Write Data Timing When the Burst Length is BL8****Write Data in 1:4 Clock Ratio**

- **wr\_data**: data bus port, and the user can use this port to write data to be stored in DDR
- **wr\_data\_en**: data write enable port, active-high
- **wr\_data\_end**: keep the same as **wr\_data\_en** signal when the clock ratio is 1:4
- **wr\_data\_rdy**: when **wr\_data\_rdy** is high, it means that the controller can receive user data, and the user can write data to the controller through **wr\_data**, **wr\_data\_en** and **wr\_data\_end**

**Figure 4-9 Write Timing in 1:4 Clock Ratio**

### 4.4.5 Read Data

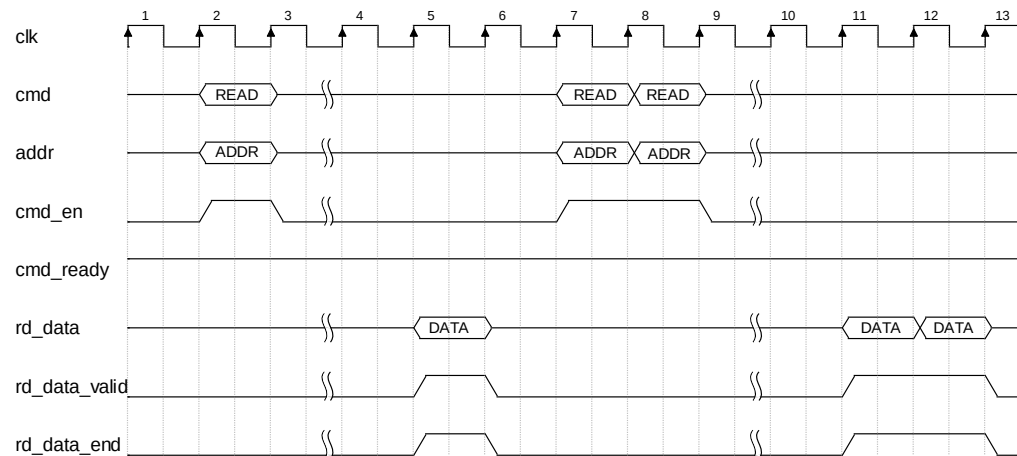
You can read the data from the DDR2 SDRAM using `rd_data`, `rd_data_valid`, and `rd_data_end`.

#### Read Data in 1:2 Clock Ratio

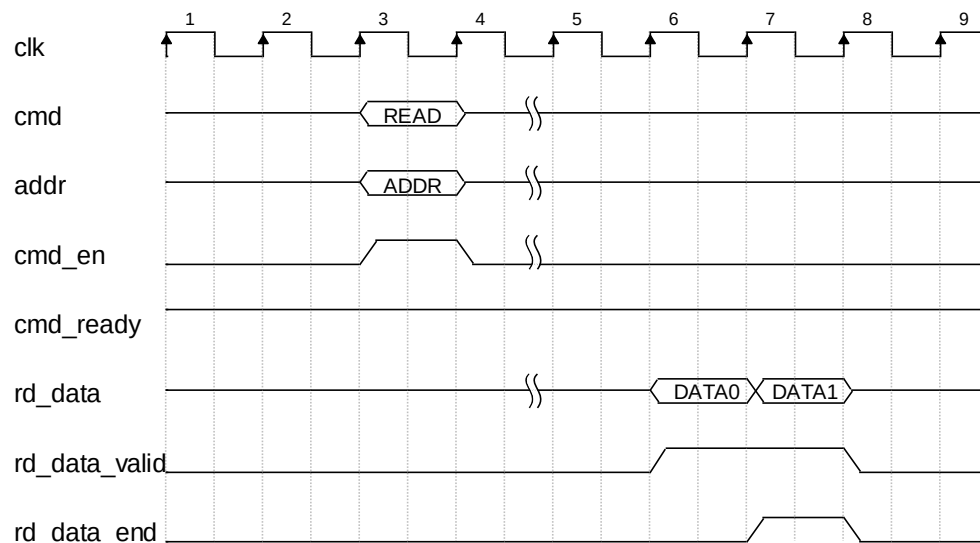
- `rd_data`: Returned read data port
- `rd_data_valid`: Read data valid port; when it is high, indicates that the returned `rd_data` is valid
- `rd_data_end`: Indicates the last set of data returned under the current burst length, active-high

When the user reads multiple addresses consecutively, the corresponding data will be returned in the order of the addresses when the read command is sent.

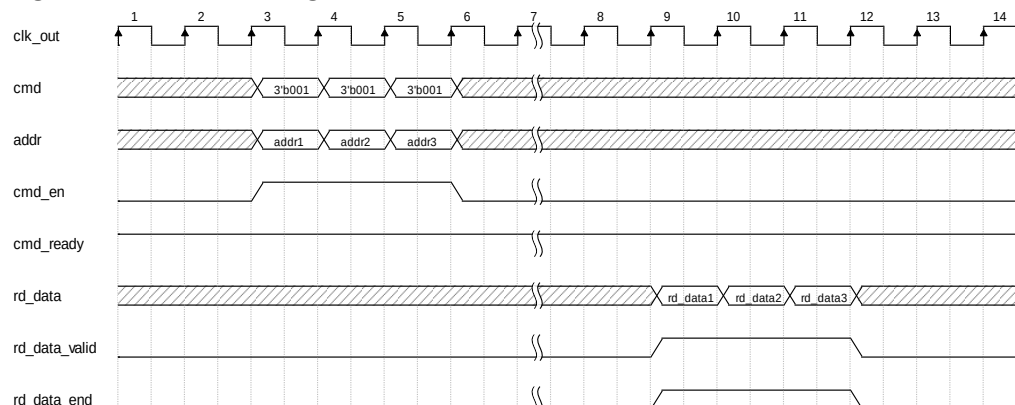
**Figure 4-10 Read Timing in 1:2 Clock Ratio**



Similar to the write operation, because the clock ratio for MC and PHY is 1:2, read data occupies two CLK cycles if the user configures a BL8 burst length, as shown in Figure 4-11.

**Figure 4-11 Read Data Timing When the Burst Length is BL8****Read Data in 1:4 Clock Ratio**

- rd\_data: Returned read data port
- rd\_data\_valid: Read data valid port; when it is high, it indicates that the returned rd\_data is valid
- rd\_data\_end: When Clock ratio 1:4, consistent with rd\_data\_valid

**Figure 4-12 Read Timing in 1:4 Clock Ratio****4.4.6 Refresh****Refresh**

The DDR2 SDRAM memory array needs to be continually refreshed to ensure the data is not lost. As such, Gowin DDR2 Memory Interface IP is required to periodically send the refresh commands to the DDR2 SDRAM. Gowin DDR2 Memory Interface IP intervals tREFI time to generate the refresh command; after the refresh command is generated, the MC executes the last read/write command, it will PreCharge all the Banks and then execute the Refresh command, the refresh operation has a higher priority.

### Self-Refresh

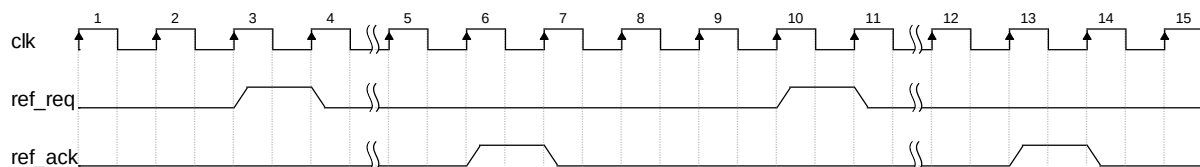
Users can send a self-refresh request through the `sr_req` port and configure the DDR2 SDRAM to enter the self-refresh mode. In the self-refresh mode, DDR2 SDRAM will automatically refresh the memory array without the need for a refresh command from Gowin DDR2 Memory Interface IP.

Gowin DDR2 Memory Interface IP will return the `sr_ack` signal to the user after the self-refresh is completed, indicating that the DDR2 SDRAM has entered the self-refresh mode.

### User Refresh

You can use the option to configure the user refresh mode, and "USER\_REFRESH" needs to be set to "ON." You can refresh via the MC at any time using the `ref_req` port without the requirement to send additional commands to the MC via the `CMD` port. When the user refresh command is sent, the `ref_req` needs to continue at a high level for one cycle. After sending the refresh command, the MC will feedback the `ref_ack` signal and maintain it at a high level for one cycle, as shown in Figure 4-13.

**Figure 4-13 User Refresh Timing**



The user refresh operation may affect commands already received or being executed by the MC. The MC will prioritize the completion of the command operation being executed before the user refresh operation. The user should consider the coordination between issuing a user refresh and the various commands to avoid causing a  $t_{REFI}$  violation.

Considering the worst case scenario, the user refresh can be operated with reference to the following formula, commanding a certain amount of time to complete the transmission, which can be roughly calculated by parameters such as  $t_{RCD}$ ,  $CL$ , data transmission time,  $t_{RP}$ , etc., and the user refresh should be completed before the violation of the time parameter  $t_{REFI}$ , so the maximum interval between the two user refreshes is approximately:

$$t_{REFI} - (t_{RCD} + (CL + 4) \times t_{CK} + t_{RP}) \times nBA$$

In the actual application, if the user refresh starts, the user will need to send a user refresh immediately after finishing the DDR2 SDRAM initialization, which will establish a time benchmark for subsequent user refresh requests.

# 5 Notes on IP Usage

## 5.1 Clock and Reset

### 5.1.1 Clock

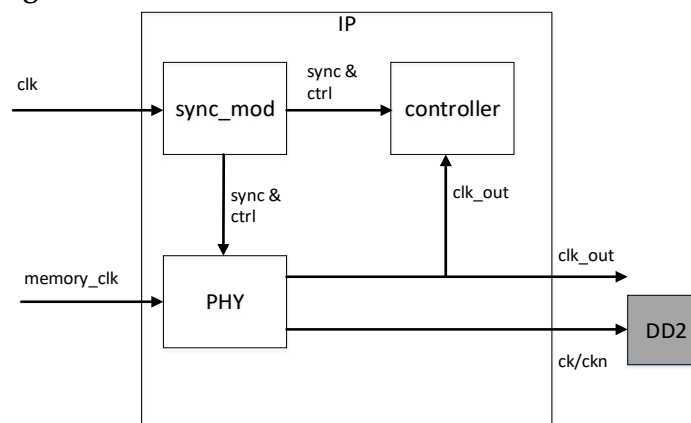
The IP has three clocks, two input clocks, `clk` and `memory_clk`, and one output clock, `clk_out`, as shown in Figure 5-1.

`clk` is a low-speed continuous clock, which is used to generate some synchronization and control signals that act on the main logic of the IP (PHY layer and Memory Controller). The recommended value is 50MHz, and you can connect the input of the on-board crystal to `clk`.

`memory_clk` is a high-speed clock that uses HCLK resources to drive the PHY and output to the DDR2 chip.

`clk_out` is the divided clock for `memory_clk`. When CLK Ratio is 1:4, `clk_out` is the quarter-frequency clock of `memory_clk`, using PCLK resources. `clk_out` is used as the logic processing clock for the IP and outputs to the user logic, and User operations on the IP interface should be synchronized with `clk_out`.

Figure 5-1 Clock



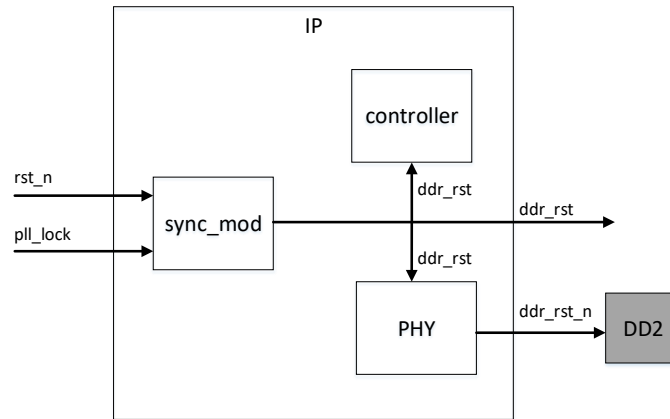
### 5.1.2 Reset

The IP has input signals `rst_n` and `pll_lock`, and output signal `ddr_rst`. As shown in Figure 5-2, `rst_n` and `pll_lock` perform an operation to generate `ddr_rst`, which serves as the global reset for the IP and is output

to the user.

Any reset logic can connect to rst\_n. pll\_lock can only connect to the LOCK signal of the PLL. If pll\_lock does not connect to the LOCK signal of the PLL, IP will not be able to detect whether the clock is stable or not, and at this time it is prone to DDR initialization failure.

Figure 5-2 Reset



## 5.2 pll\_stop

pll\_stop is a control signal present in the GW5A(S)(T) device and is a switch that controls memory\_clk, active-low.

For 138K devices, pll\_stop is connected directly to enclk2 of the PLL, as shown in Figure 5-3.

For 25K devices, pll\_stop needs to be connected to the conversion & connection module pll\_mDRP\_intf to indirectly control the PLL's clkout2. pll\_mDRP\_intf module's clk is the same as the PLL's mdclk and clkin, as shown in Figure 5-4.

Figure 5-3 138K pll\_stop

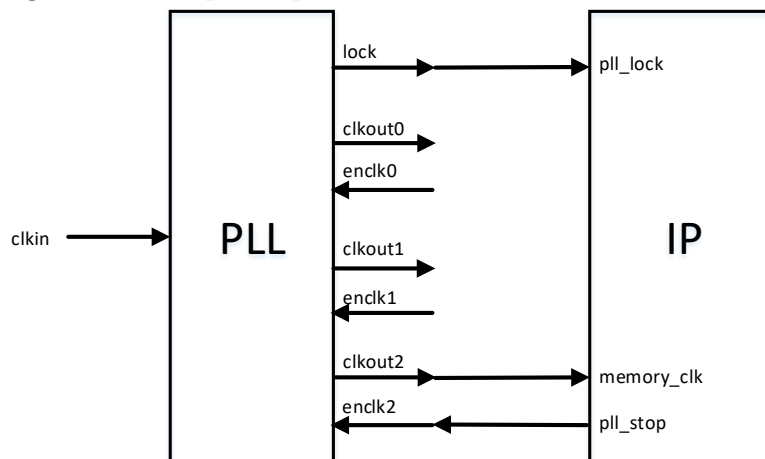
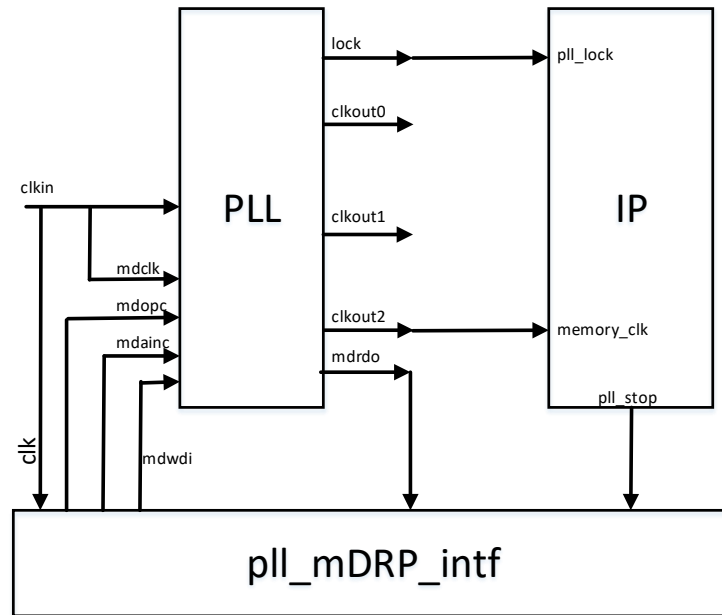


**Figure 5-4 25K pll\_stop**

# 6 Port List

The I/O port of Gowin DDR2 Memory Interface IP is shown in Table 6-1.

**Table 6-1 I/O List of Gowin DDR2 Memory Interface IP**

| Signal         | Data Width     | I/O    | Description                                                                                             |
|----------------|----------------|--------|---------------------------------------------------------------------------------------------------------|
| User Interface |                |        |                                                                                                         |
| addr           | ADDR_WIDTH     | Input  | Address signal width                                                                                    |
| cmd            | 3              | Input  | Command channel                                                                                         |
| cmd_en         | 1              | Input  | Command and address enable signals:<br>0: invalid<br>1: valid                                           |
| cmd_ready      | 1              | Output | Indicate the memory interface is ready to receive commands and addresses at a high level                |
| rd_data        | APP_DATA_WIDTH | Output | Read data channel                                                                                       |
| rd_data_end    | 1              | Output | When at a high level, it indicates the end of the current output cycle for the group of rd_data         |
| rd_data_valid  | 1              | Output | rd_data valid signal:<br>0: invalid<br>1: valid                                                         |
| burst          | 1              | Input  | Reserved, input the fixed 0                                                                             |
| wr_data        | APP_DATA_WIDTH | Input  | Write data channel                                                                                      |
| wr_data_end    | 1              | Input  | When at a high level, it indicates that the current clock cycle is the last cycle for the group of data |
| wr_data_mask   | APP_MASK_WIDTH | Input  | Provide the mask signals for wr_data                                                                    |
| wr_data_rdy    | 1              | Output | MC is ready to receive the user data at a high level                                                    |
| wr_data_en     | 1              | Input  | wr_data enable signal:<br>0: invalid<br>1: valid                                                        |
| sr_req         | 1              | Input  | Self-refresh request                                                                                    |

| Signal               | Data Width        | I/O    | Description                                                                                                                                                                                                                                     |
|----------------------|-------------------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| sr_ack               | 1                 | Output | Self-refresh acknowledgment signal                                                                                                                                                                                                              |
| ref_req              | 1                 | Input  | User refresh request                                                                                                                                                                                                                            |
| ref_ack              | 1                 | Output | User refresh acknowledgment signal                                                                                                                                                                                                              |
| clk                  | 1                 | Input  | Reference input clock, typically PCB crystal oscillator input, recommended 50MHz crystal oscillator                                                                                                                                             |
| memory_clk           | 1                 | Input  | Chip operating clock input by user, generally a high-speed clock from the PLL multiplication; for GW2A devices, this clock can be the output clock of the PLL or other clock; for GW5A devices, this clock must be output by clkout2 of the PLL |
| pll_stop             | 1                 | Output | You can see <a href="#">5.2 pll_stop</a> for details                                                                                                                                                                                            |
| pll_lock             | 1                 | Input  | If memory_clk is PLL multiplication input, this port is connected to pll_lock pin of PLL; if user does not use PLL, this port is connected to 1'b1                                                                                              |
| rst_n                | 1                 | Input  | Reset input, active-low                                                                                                                                                                                                                         |
| ddr_rst              | 1                 | Output | The reset signal processed by the IP for user design, active-high                                                                                                                                                                               |
| init_calib_complete  | 1                 | Output | Initialization complete signal                                                                                                                                                                                                                  |
| clk_out              | 1                 | Output | User design clock<br>For clock ratio 1:2, the frequency is 1/2 of Memory Clk;<br>For clock ratio 1:4, frequency is 1/4 of Memory Clk                                                                                                            |
| ecc_err              | APP_DATA_WIDTH/32 | Output | ECC indicator signal output                                                                                                                                                                                                                     |
| dbg_vector1_out      | 3*DQS_WIDTH       | Output | Debug port, used only when debug port is enabled.                                                                                                                                                                                               |
| dbg_vector2_out      | 2*DQS_WIDTH       | Output | Debug port, used only when debug port is enabled.                                                                                                                                                                                               |
| dbg_vector3_out      | 8                 | Output | Debug port, used only when debug port is enabled.                                                                                                                                                                                               |
| DDR2 SDRAM Interface |                   |        |                                                                                                                                                                                                                                                 |
| O_dds_addr           | ROW_WIDTH         | Output | Row address (activation command), Column address (read/write command)                                                                                                                                                                           |
| O_dds_ba             | BANK_WIDTH        | Output | Bank address                                                                                                                                                                                                                                    |
| O_dds_cs_n           | CS_WIDTH          | Output | Chip selected, active-low.                                                                                                                                                                                                                      |
| O_dds_ras_n          | 1                 | Output | Column address strobe signal                                                                                                                                                                                                                    |
| O_dds_cas_n          | 1                 | Output | Column address selects the communication No.                                                                                                                                                                                                    |
| O_dds_we_n           | 1                 | Output | Row write enable                                                                                                                                                                                                                                |
| O_dds_clk            | CK_WIDTH          | Output | A clock signal provided for DDR2 SDRAM                                                                                                                                                                                                          |

| Signal        | Data Width | I/O         | Description                                |
|---------------|------------|-------------|--------------------------------------------|
| O_ddr_clk_n   | CK_WIDTH   | Output      | Compose a differential signal with ddr_ck  |
| O_ddr_cke     | CKE_WIDTH  | Output      | DDR2 SDRAM clock enable signal             |
| O_ddr_dqm     | DM_WIDTH   | Output      | DDR2 SDRAM data mask signal                |
| O_ddr_odt     | ODT_WIDTH  | Output      | Memory signal termination resistor control |
| O_ddr_reset_n | 1          | Output      | DDR2 SDRAM reset signal                    |
| IO_ddr_dq     | DQ_WIDTH   | Bidirection | DDR2 SDRAM data                            |
| IO_ddr_dqs    | DQS_WIDTH  | Bidirection | DDR2 SDRAM data strobe signal              |
| IO_ddr_dqs_n  | DQS_WIDTH  | Bidirection | Compose a differential signal with ddr_dqs |

# 7 Parameter Configuration

Gowin DDR2 Memory Interface IP supports DDR2 SDRAM devices. You need to configure the static and timing parameters of Gowin DDR2 Memory Interface according to the design requirements, as shown in Table 7-1 and Table 7-2.

## Parameters in 1:2 Clock Ratio

**Table 7-1 Static Parameter Options of Gowin DDR2 Memory Interface**

| Name           | Description                               | Option                                          |
|----------------|-------------------------------------------|-------------------------------------------------|
| DRAM_TYPE      | Memory type                               | DDR2                                            |
| DRAM_WIDTH     | DQ width of DDR2 chip                     | 4, 8, 16                                        |
| ADDR_CMD_MODE  | Address command mode                      | 1T, 2T                                          |
| nCK_PER_CLK    | Clock ratio between PHY and MC interfaces | 2.                                              |
| nCS_PER_RANK   | The number of each Rank CS                | 1                                               |
| APP_ADDR_WIDTH | Address width                             | RANK_WIDTH + BANK_WIDTH + ROW_WIDTH + COL_WIDTH |
| BANK_WIDTH     | Memory BANK address width                 | Select according to the DDR2 SDRAM chip         |
| CS_WIDTH       | CS bit width                              | Select according to the DDR2 SDRAM chip         |
| RANK_WIDTH     | RANK address width                        | Select 1 for single and dual rank devices       |
| ROW_WIDTH      | DRAM ROW address width                    | Select according to the DDR2 SDRAM chip         |
| DM_WIDTH       | Data mask bit width                       | DQ_WIDTH/ DRAM_WIDTH                            |
| DQ_WIDTH       | DQ signal width                           | DQ_WIDTH=DRAM_WIDTH * DQS_WIDTH                 |
| DQS_WIDTH      | DQS signal width                          | DQ_WIDTH/8                                      |
| BURST_MODE     | Burst length                              | "4", "8"                                        |
| BURST_TYPE     | Data read and write when bursting         | "Sequential" "Interleaved"                      |
| RTT_NOM        | Nominal ODT value                         | "150": 150                                      |

| Name           | Description                                                                                         | Option                                                                     |
|----------------|-----------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------|
|                |                                                                                                     | "75": 75<br>"50": 50                                                       |
| RTT_WR         | Dynamic ODT value used for write port in Multiple-RANK; for Single-Component design, RTT_WR invalid | "OFF": RTT_WR disabled.<br>"120": RZQ/2<br>"60": RZQ/4                     |
| APP_DATA_WIDTH | User interface data signal width                                                                    | $APP\_DATA\_WIDTH = 2 * nCK\_PER\_CLK * DQ\_WIDTH$                         |
| APP_MASK_WIDTH | User interface Mask signal width                                                                    | $APP\_DATA\_WIDTH/DRAM\_WIDTH$                                             |
| USER_REFRESH   | User refresh                                                                                        | "ON", "OFF"                                                                |
| DBG_PARAMETER1 | Debug parameter                                                                                     | 000/001/010/011/100/101/110/111, used only when debug parameter is enabled |
| DBG_PARAMETER2 | Debug parameter                                                                                     | 0~127, used only when debug parameter is enabled                           |
| DBG_PARAMETER3 | Debug parameter                                                                                     | 0~127, used only when debug parameter is enabled                           |
| DBG_PARAMETER4 | Debug parameter                                                                                     | 0~127, used only when debug parameter is enabled                           |

Table 7-2 DDR2 Time Parameters

| Name       | Description                                                                                                                                                                      |
|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $t_{CK}$   | Memory interface clock period (ps)                                                                                                                                               |
| $t_{CKE}$  | Minimum pulse time of CKE signal (ps)                                                                                                                                            |
| $t_{FAW}$  | In the same rank, the interval time for sending more than four row activation commands simultaneously; therefore, the minimum value should not be less than four times $t_{RRD}$ |
| $t_{RAS}$  | Time from ACTIVE to PRECHARGE                                                                                                                                                    |
| $t_{RCD}$  | Time from ACTIVE to READ/WRITE                                                                                                                                                   |
| $t_{REFI}$ | Memory refresh interval                                                                                                                                                          |
| $t_{RFC}$  | The interval from REFRESH to ACTIVE/REFRESH.                                                                                                                                     |
| $t_{RP}$   | PRECHARGE cycle                                                                                                                                                                  |
| $t_{RRD}$  | The interval from ACTIVE to ACTIVE                                                                                                                                               |
| $t_{RTP}$  | The interval from READ to PRECHARGE                                                                                                                                              |
| $t_{WTR}$  | The interval from WRITE to READ                                                                                                                                                  |
| AL         | Additive latency                                                                                                                                                                 |
| CL         | CAS latency                                                                                                                                                                      |
| WR_CYC     | Write recovery for auto precharge                                                                                                                                                |

**Parameters in 1: 4 Clock Ratio****Table 7-3 Parameters in 1: 4 Clock Ratio**

| Name             | Description                                                                     | Option                                                |
|------------------|---------------------------------------------------------------------------------|-------------------------------------------------------|
| Memory Type      | Memory type                                                                     | M14D2561616A-2.5BG2E<br>Custom                        |
| Memory Clock     | Chip interface clock frequency                                                  | Write according to chip<br>operating clock and demand |
| CLK Ratio        | Ratio of user interface clock<br>frequency to chip interface clock<br>frequency | 1:4                                                   |
| DIMM Type        | DIMM type                                                                       | Components、RDIMMs、<br>UDIMMs、SODIMMs                  |
| Dq Width         | Dq data width                                                                   | 8, 16, 24, 32, 40, 48, 56, 64                         |
| Dram Width       | Data bit width for single memory<br>chip                                        | 8, 16                                                 |
| Rank Address     | Rank address                                                                    | Select 1 for single and dual<br>rank devices          |
| Bank Address     | Memory BANK address width                                                       | Select according to the DDR2<br>SDRAM chip            |
| Row Address      | Memory row address width                                                        | Select according to the DDR2<br>SDRAM chip            |
| Column Address   | Memory column address width                                                     | Select according to the DDR2<br>SDRAM chip            |
| Burst Mode       | Memory chip burst mode                                                          | 8                                                     |
| Burst Type       | Memory chip burst type                                                          | SEQ: Sequential<br>INT: Interleaved                   |
| CAS Latency      | CAS latency                                                                     | 2, 3, 4, 5, 6                                         |
| Additive Latency | Additive latency                                                                | 0, 1, 2, 3, 4, 5                                      |
| Write Recovery   | CWL latency                                                                     | 2, 3, 4, 5, 6                                         |
| RTT NOM          | Nominal ODT value                                                               | OFF, 150, 75, 50                                      |
| Addr Cmd Mode    | Address command mode                                                            | 1T, 2T                                                |
| USER<br>REFRESH  | User refresh                                                                    | Checked: Enable<br>Unchecked: Disable                 |

Refer to Table 7-2 for time parameters.

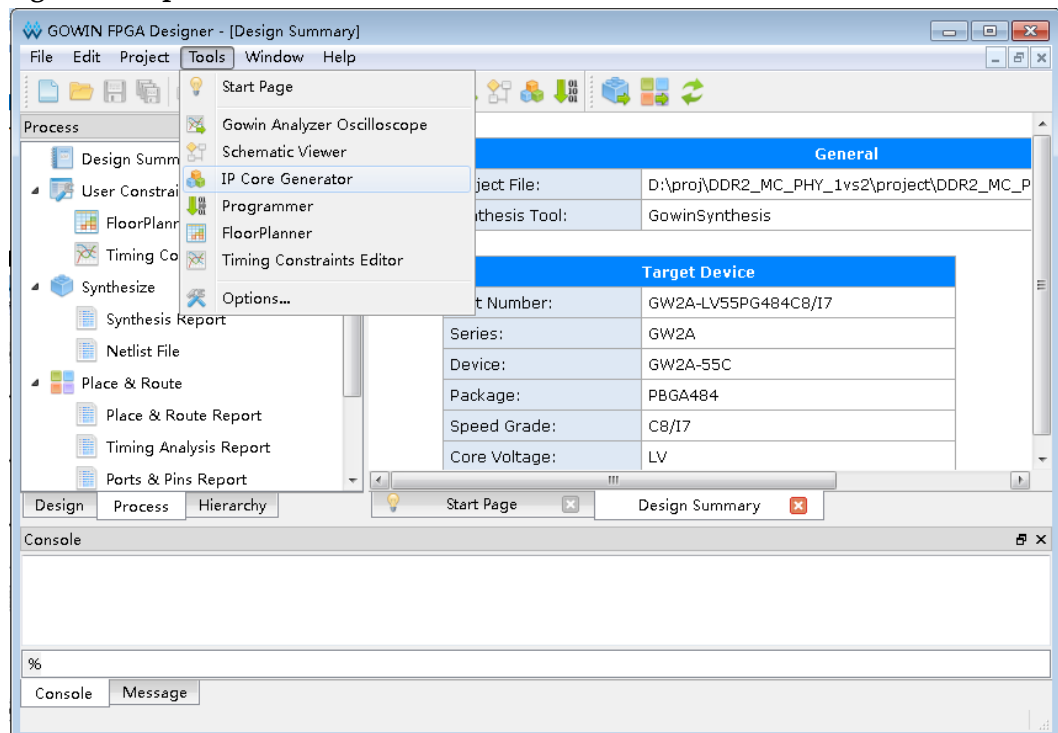
# 8 Interface Configuration

You can invoke and configure Gowin DDR2 Memory Interface IP through the IP Core Generator tool in the IDE. In this chapter, we take MT47H64M16-3 memory as an example. We introduce the configuration interface and configuration flow, and explain the meaning of each configuration option.

## 1. Open the IP Core Generator

After creating the project, click on the Tools option and select the IP Core Generator via the drop-down list to open IP Core Generator, as shown in Figure 8-1.

**Figure 8-1 Open IP Core Generator**

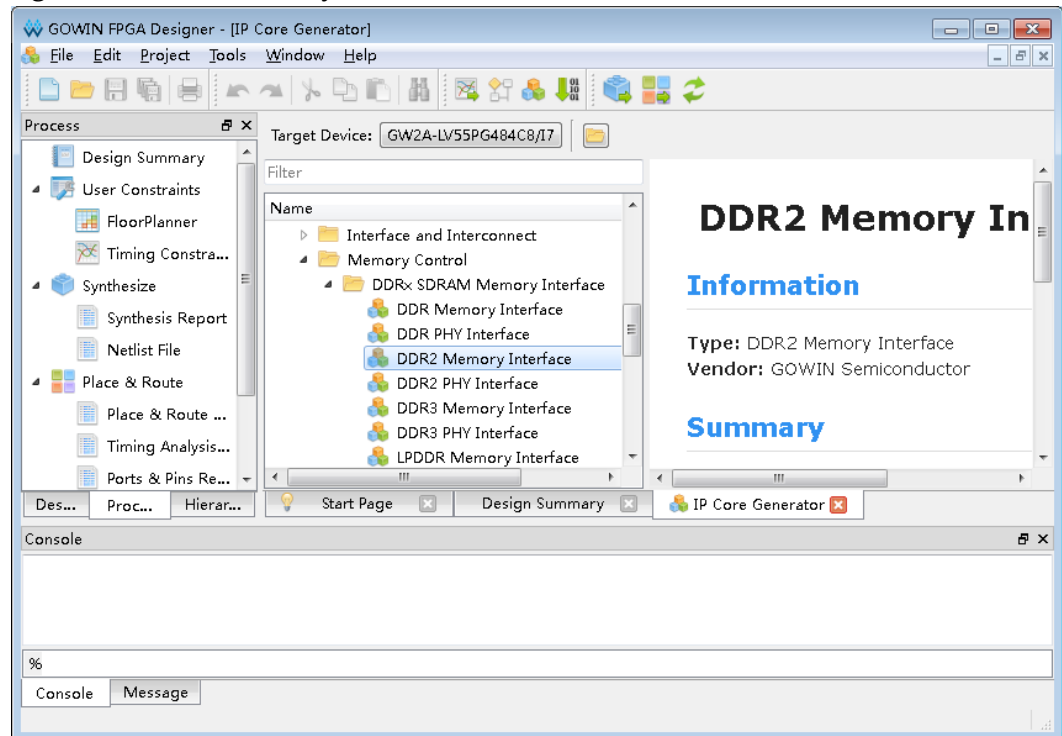


## 2. Open DDR2 Memory Interface IP core

Click on "DDR<sub>x</sub> SDRAM Memory Interface" option and double-click on DDR2 Memory Interface; the DDR2 Memory Interface IP core will open, as

shown in Figure 8-2.

**Figure 8-2 DDR2 Memory Interface IP core**

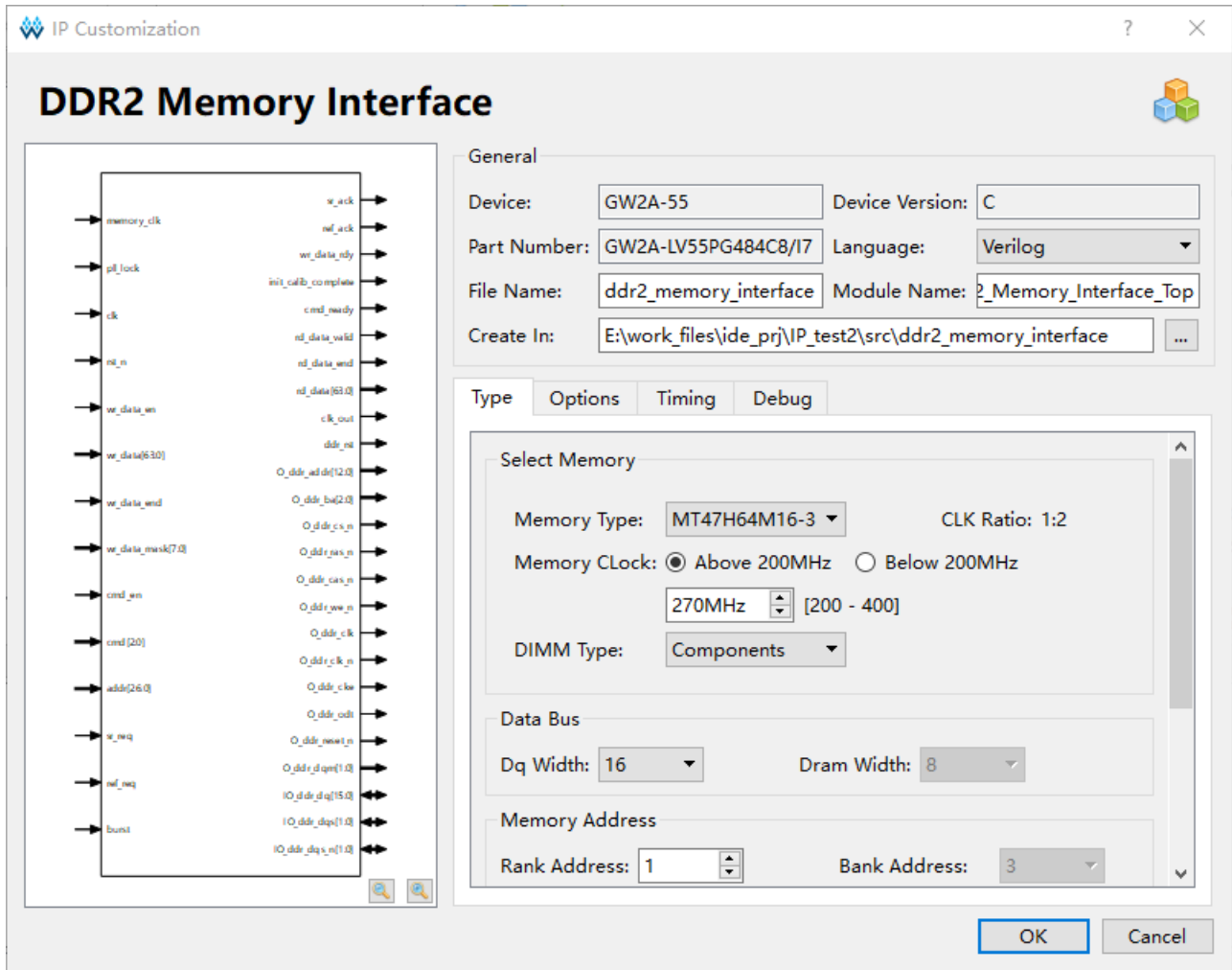


### 3. DDR2 Memory Interface IP Core Ports

The ports diagram of the DDR2 Memory Interface IP core is on the left, as shown in Figure 8-3.

The left side is the interface between the DDR2 Memory Controller and the user side. You can connect your design to the DDR2 Memory Interface IP to send/receive commands and data. The right side is the interface between the physical interface (PHY) and memory chip. You can access data by connecting the DDR2 Memory Interface IP core and the memory chip. The signal bit-width and number will change according to the configuration options.

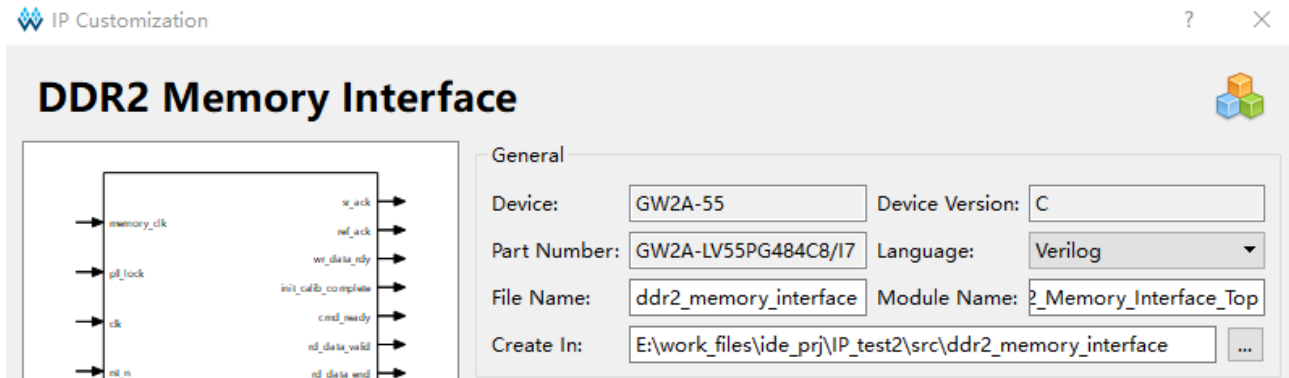
Figure 8-3 IP Core Interface



#### 4. Configure Basic Information

See the basic information configuration in the upper part of the configuration interface. Take GW2A-55C chip and PBGA484 package as an example; the module name option displays the top-level file name after the project is generated, and the default is "DDR2\_Memory\_Interface\_Top"; you can modify this name. "File Name" displays the folder generated by the IP core file. The files of the DDR2 Memory Interface IP core are stored in this path. The default is "ddr2\_memory\_interface", and you can modify the path. The "Create In" option displays the path generated by the IP core folder. The default is "\project path\src\ddr2\_memory\_interface ", and you can modify the path.

Figure 8-4 Basic Information Configuration Interface



### 5. Type Tab

In the Type tab, you need to configure the basic information for the DDR2 memory chip.

- Select Memory
- Data Bus
- Memory Address

You can fill in the address information for the Rank, Bank, Row, and Column of the DDR2 memory chip. After you select the DDR2, the memory address options in the GUI will be automatically completed. If you choose the Custom option, you need to choose the parameters according to the DDR2 Memory type.

Figure 8-5 Type Tab

**IP Customization**

## DDR2 Memory Interface

**General**

Device: GW2A-55 Device Version: C

Part Number: GW2A-LV55PG484C8/I7 Language: Verilog

File Name: ddr2\_memory\_interface Module Name: 2\_Memory\_Interface\_Top

Create In: E:\work\_files\ide\_prj\IP\_test2\src\ddr2\_memory\_interface

**Type** Options Timing Debug

**Select Memory**

Memory Type: MT47H64M16-3 CLK Ratio: 1:2

Memory Clock: ☒ Above 200MHz ☐ Below 200MHz

270MHz [200 - 400]

DIMM Type: Components

**Data Bus**

Dq Width: 16 Dram Width: 8

**Memory Address**

Rank Address: 1 Bank Address: 3

Row Address: 13 Column Address: 10

Addr Width: 27

Data Width: 64

Mask Width: 8

☐ Ecc

OK Cancel

### 6. Options Tab

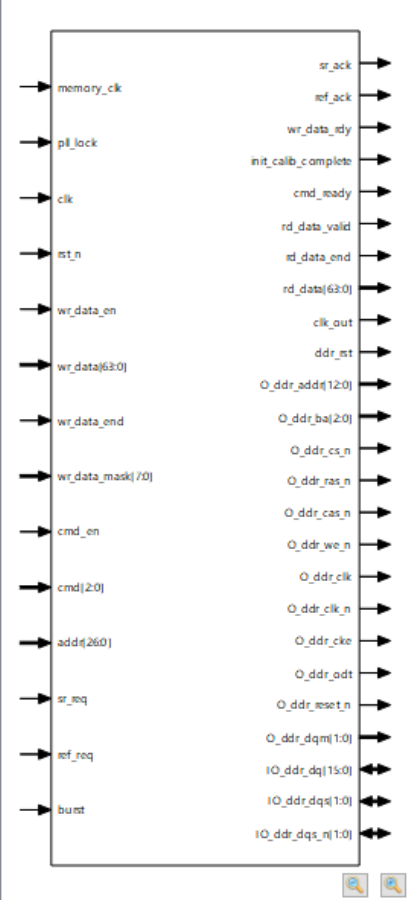
- Memory Options
- Mode Register Setting
- Generation Config Option

In the generated IP, if it is checked, the primitives such as IBUF, OBUF are not inserted, and the port is directly connected to the logic; it is checked by default.

Figure 8-6 Options Tab

IP Customization

## DDR2 Memory Interface



**General**

Device: GW2A-55 Device Version: C

Part Number: GW2A-LV55PG484C8/I7 Language: Verilog

File Name: ddr2\_memory\_interface Module Name: DR2\_Memory\_Interface\_Top

Create In: E:\work\_files\ide\_prj\IP\_test2\src\ddr2\_memory\_interface

**Options**

**Memory Options**

Burst Mode: 4

Burst Type: SEQ

☐ User Refresh

**Mode Register Setting**

CAS Latency: 4 Additive Latency: 0

Write Recovery: 6 Rtt Nom: OFF

Addr Cmd Mode: 1T OUTPUT DRV: Full strength

☒ DDR2 DQSN Enable

**Generation Config**

☒ Disable I/O Insertion

OK Cancel

### 7. Timing Tab

- Command and Address Timing Option
- Refresh, Reset and Power Timing option

Figure 8-7 Timing Tab

IP Customization

## DDR2 Memory Interface

memory\_clk

pll\_lock

clk

rst\_n

wr\_data\_en

wr\_data[63:0]

wr\_data\_end

wr\_data\_mask[7:0]

cmd\_en

cmd[2:0]

add[26:0]

sr\_req

ref\_req

bunt

sr\_ack

ref\_ack

wr\_data\_idy

init\_calib\_c\_complete

cmd\_ready

rd\_data\_valid

rd\_data\_end

rd\_data[63:0]

clk\_out

ddr\_rst

O\_ddr\_add[12:0]

O\_ddr\_ba[2:0]

O\_ddr\_cs\_n

O\_ddr\_ras\_n

O\_ddr\_cas\_n

O\_ddr\_we\_n

O\_ddr\_clk

O\_ddr\_clk\_n

O\_ddr\_cke

O\_ddr\_odt

O\_ddr\_reset\_n

O\_ddr\_dqm[1:0]

IO\_ddr\_dq[15:0]

IO\_ddr\_dqs[1:0]

IO\_ddr\_dqs\_n[1:0]

General

Device: GW2A-55 Device Version: C

Part Number: GW2A-LV55PG484C8/I7 Language: Verilog

File Name: ddr2\_memory\_interface Module Name: DR2\_Memory\_Interface\_Top

Create In: E:\work\_files\ide\_prj\IP\_test2\src\ddr2\_memory\_interface

Type Options Timing Debug

Command and Address Timing

tRTP Period: 7500ps tRP Period: 12500ps

tWTR Period: 7500ps tRC Period: 55000ps

tRAS Period: 37500ps tRCD Period: 12500ps

tFAW Period: 40000ps tRRD Period: 7500ps

Refresh Reset and Power Down Timing

tCKE Period: 75000ps tREFI Period: 7800000ps

tRFC Period: 160000ps tDLLK: 512

OK Cancel

### 8. Debug Option

Debug tab is as shown in Figure 8-8. If it is checked, you can see debug parameters and debug ports.

Figure 8-8 Debug Tab

IP Customization

## DDR2 Memory Interface

memory\_clk

pll\_lock

clk

rst\_n

wr\_data\_en

wr\_data[63:0]

wr\_data\_end

wr\_data\_mask[7:0]

cmd\_en

cmd[2:0]

add[26:0]

sr\_req

ref\_req

burst

sr\_ack

ref\_ack

wr\_data\_rdy

init\_calib\_c\_complete

cmd\_ready

rd\_data\_valid

rd\_data\_end

rd\_data[63:0]

clk\_out

ddr\_rst

O\_ddr\_add[12:0]

O\_ddr\_ba[2:0]

O\_ddr\_cs\_n

O\_ddr\_ras\_n

O\_ddr\_cas\_n

O\_ddr\_we\_n

O\_ddr\_clk

O\_ddr\_clk\_n

O\_ddr\_cke

O\_ddr\_odt

O\_ddr\_reset\_n

O\_ddr\_dqm[1:0]

IO\_ddr\_dq[15:0]

IO\_ddr\_dqs[1:0]

IO\_ddr\_dqs\_n[1:0]

General

Device: GW2A-55 Device Version: C

Part Number: GW2A-LV55PG484C8/I7 Language: Verilog

File Name: ddr2\_memory\_interface Module Name: DR2\_Memory\_Interface\_Top

Create In: E:\work\_files\ide\_prj\IP\_test2\src\ddr2\_memory\_interface

Type Options Timing Debug

☐ Debug Parameter Enable

Debug Parameter1 Value: 101

Debug Parameter2 Value: 0 (0-127)

Debug Parameter3 Value: 0 (0-127)

Debug Parameter4 Value: 0 (0-127)

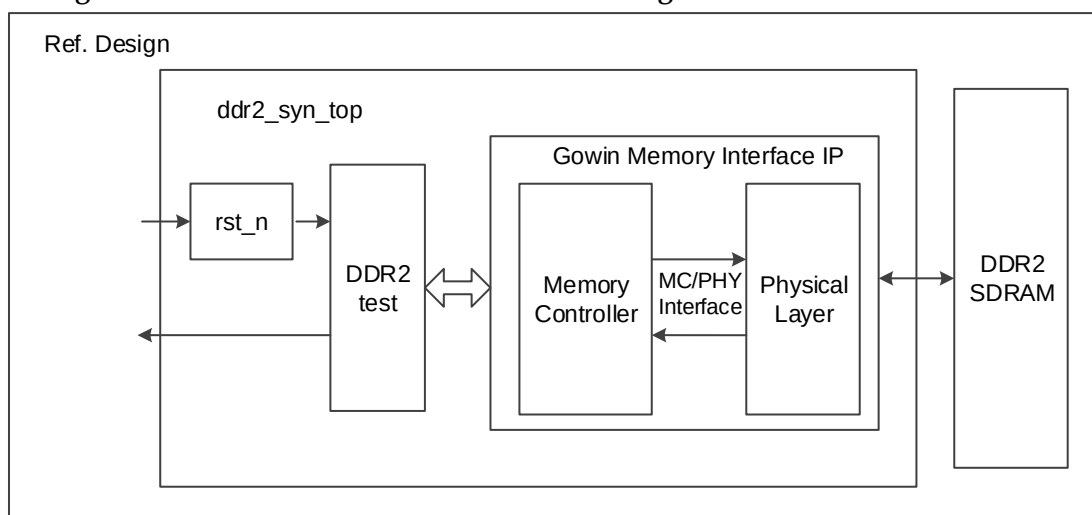
☐ Debug Port Enable

OK Cancel

# 9 Reference Design

To help users quickly familiarize themselves with Gowin DDR2 memory interface IP, a simple [reference design](#) is provided. The basic structure of this reference is shown in Figure 9-1.

**Figure 9-1 Basic Structure of the Reference Design**



In the reference design, the `ddr2_syn_top` module is the top-level module, and its ports are connected to the input reference clocks, external reset signals, etc. The connection is shown in Table 9-1. The `DDR2_test` is used to generate the address, data, and read/write commands required by Gowin Memory Interface IP, and the module can be synthesized.

**Table 9-1 DDR2\_syn\_top Module Input Interface List**

| Name  | Description                              |
|-------|------------------------------------------|
| clk   | Input reference clock, 50 MHz by default |
| rst_n | Input reset signal                       |

The `DDR2_test` performs write and read operations for different addresses. You can modify the written address and data, etc., and analyze and verify the read data received from the Memory Interface IP. In the reference design, you can select the part number MT47H64M16-3,

configure the Burst Mode as BC4, and set the DQ width to 16 bits.

The simulation waveforms of some signals between the DDR2\_test and Memory Interface IP interfaces are shown in Figure 9-2.

### Figure 9-2 Part of the DDR2\_test Port Signal Simulation Waveform



# 10 File Delivery

The delivery file for Gowin DDR2 Memory Interface IP includes documents and reference design.

## 10.1 Document

The folder contains PDF version for the user guide.

**Table 10-1 File List**

| Name                                               | Description                                |
|----------------------------------------------------|--------------------------------------------|
| IPUG506, Gowin DDR2 Memory Interface IP User Guide | Gowin DDR2 Memory Interface IP User Manual |

## 10.2 Reference Design

The Ref. Design folder contains the netlist file, user reference design, constraint file, jitter elimination module, top file, and project folder of Gowin DDR2 Memory Interface IP.

**Table 10-2 Ref. Design Folder Contents List**

| Name                     | Description                                 |
|--------------------------|---------------------------------------------|
| ddr2_syn_top.v           | The top module of the reference design      |
| DDR2_test.v              | Test stimulus generation module             |
| DDR2_Memory_Interface.vo | Gowin DDR2 memory interface IP netlist file |
| ddr2.cst                 | DDR2 project physical constraint file       |
| ddr2.sdc                 | DDR2 project timing constraint file         |
| DDR2_Memory_Interface    | DDR2 IP project folder                      |

