



Gowin DDR Memory Interface IP User Guide

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Revision History

Date	Version	Description
12/18/2017	1.0E	Initial version.
03/06/2018	1.1E	The manual content improved, the descriptions of functions, port lists, parameter configurations, reference designs, interface configurations, and file delivery added.
10/25/2018	1.2E	The read and write timing diagram and the user interface updated.
07/25/2019	1.3E	● Address format modified. ● Description of read/write efficiency added.
09/25/2019	1.4E	The write data timing when the burst length is BL8 updated.
01/06/2020	1.5E	Figure 3-5 Command, Address, and Enable Signal Timing updated.
05/09/2020	1.6E	Parameters updated.
07/28/2022	1.7E	● User interfaces updated. ● Debug parameters and ports added.
12/31/2025	1.8E	● GW1N(S)(R) devices supported. ● Descriptions of chapter 4 Port List updated.

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1 About This Guide

1.1 Purpose

Gowin DDR Memory Interface IP user guide mainly includes the descriptions of structure and function, port, timing, configuration & call, reference design, etc. The guide helps you quickly learn the features and usage of Gowin DDR Memory Interface IP.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- [DS102, GW2A series of FPGA Products Data Sheet](#)
- [DS226, GW2AR series of FPGA Products Data Sheet](#)
- [DS961, GW2ANR series of FPGA Products Data Sheet](#)
- [DS100, GW1N series of FPGA Products Data Sheet](#)
- [DS117, GW1NR series of FPGA Products Data Sheet](#)
- [DS821, GW1NS series of FPGA Products Data Sheet](#)
- [SUG100, Gowin Software User Guide](#)

1.3 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminology

Abbreviations and Terminology	Full Name
FIFO	First Input First Output
IP	Intellectual Property
RAM	Random Access Memory
LUT	Look-up Table
GSR	Global System Reset
ECC	Error Correcting Code

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If any questions, comments, or suggestions, please feel free to contact us directly.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Features & Performance

Gowin DDR Memory Interface IP is a commonly used DDR interface IP, in compliance with JESD79-F. The IP includes the DDR Memory Controller (MC) and the corresponding Physical Interface (PHY) design. Gowin DDR Memory Interface IP provides the user a generic command interface to connect with the memory chip to access and store.

Table 2-1 Gowin DDR Memory Interface IP

Gowin DDR Memory Interface IP	
Logic Resource	Please refer to Table 2-2
Delivered Files	
Design Files	Verilog (encrypted)
Reference Designs	Verilog
TestBench	Verilog
Test and Design Flow	
Integrated Software	GowinSynthesis
Application Software	Gowin Software (V1.9.8.01 and above)

Note!

For the devices supported, you can click [here](#) to get the information.

2.1 Key Features

- Support GW1N(S)(R), GW2A-18, GW2AR-18, and GW2A-55 devices
- Supports industry-standard DDR SDRAM devices and modules compliant with the JESD79-F specification
- Supports selectable clock ratios of 1:1 1:2 between the DDR MC and PHY
- Supports memory data path widths of 8, 16, 24, 32, 40, 48, 56, 64, and 72 bits
- Supports memory devices with x4, x8, and x16 data widths
- Programmable burst lengths: BL2/4/8 for 1:1, and BL4/8 for 1:2 mode
- Support ECC
- Configurable CL

- Configurable AL
- Configurable t_{FAW}
- Configurable t_{RAS}
- Configurable t_{RCD}
- Configurable t_{RFC}
- Configurable t_{RRD}
- Configurable t_{RTP}
- Configurable t_{WTR}
- Supports automatically refreshing and user-initiated refreshing, with programmable auto-refresh intervals

2.2 Working Frequency

Gowin DDR Memory Interface IP supports the following DDR SDRAM data rate:

- Support 200 Mbps, and 266 Mbps when the clock rate is 1:1.
- Support 200 Mbps, 266 Mbps, 333 Mbps, and 400 Mbps when the clock rate is 1:2.

The bandwidth efficiency that Gowin DDR Memory Interface IP supports:

- The bandwidth efficiency is 50% when the clock ratio is 1:1 and the burst length is 2.
- The bandwidth efficiency is 90% when the clock ratio is 1:1 and the burst length is 4.
- The bandwidth efficiency is 90% when the clock ratio is 1:1 and the burst length is 8.
- The bandwidth efficiency is 50% when the clock ratio is 1:2 and the burst length is 4.
- The bandwidth efficiency is 90% when the clock ratio is 1:2 and the burst length is 8.

2.3 Resource Utilization

Gowin DDR Memory Interface IP is achieved via the Verilog language, which is applied for the FPGA of GW2A-55 and GW2A-18. The utilization of its resource is as shown in Table 2-2; for other application validation, please see the later release information.

Table 2-2 Resource Utilization

DDR Resource Utilization Statistics								
IP Name	LUT	ALU	SSRAM	Register	BSRAM	PLL	DLL	DQCE
DDR 1:1 MC+PHY	1061	95	44	883	0	1	1	1
DDR 1:1 PHY	411	40	21	339	0	1	1	1
DDR 1:2 MC+PHY	1122	84	83	1229	0	1	1	1
DDR 1:2 PHY	442	48	43	417	0	1	1	1

Note!

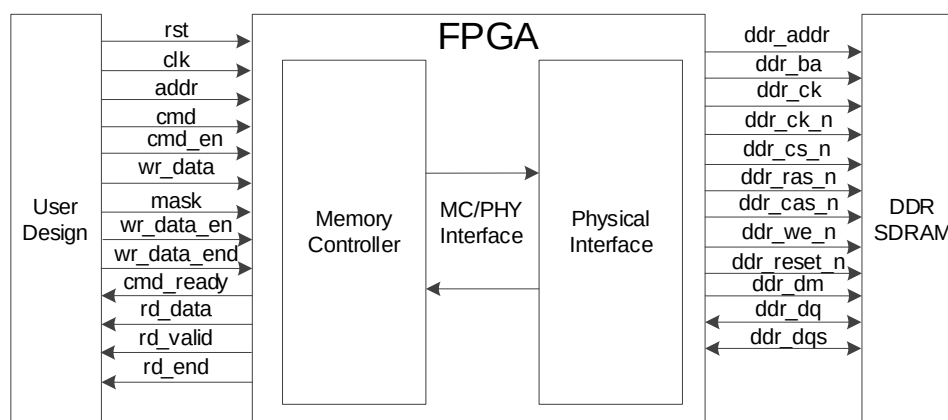
In Table 2-2, Gowin DDR Memory Interface configures the user address width to 25 bits, and DRAM WITDH x8.

3 Functions

3.1 Structure

Gowin DDR Memory Interface IP mainly includes Memory Controller, Physical Interface and other modules, and its basic structure is as shown in Figure 3-1. User Design in Figure 3-1 is the User Design connected to the external DDR SDRAM chip in FPGA.

Figure 3-1 Gowin Memory Interface IP Structure



3.2 Memory Controller

The Memory Controller is the main logic module of Gowin DDR Memory Interface IP, which locates between User Design and PHY. The Memory Controller receives the command, address, and data from the user interface and saves them in logical order.

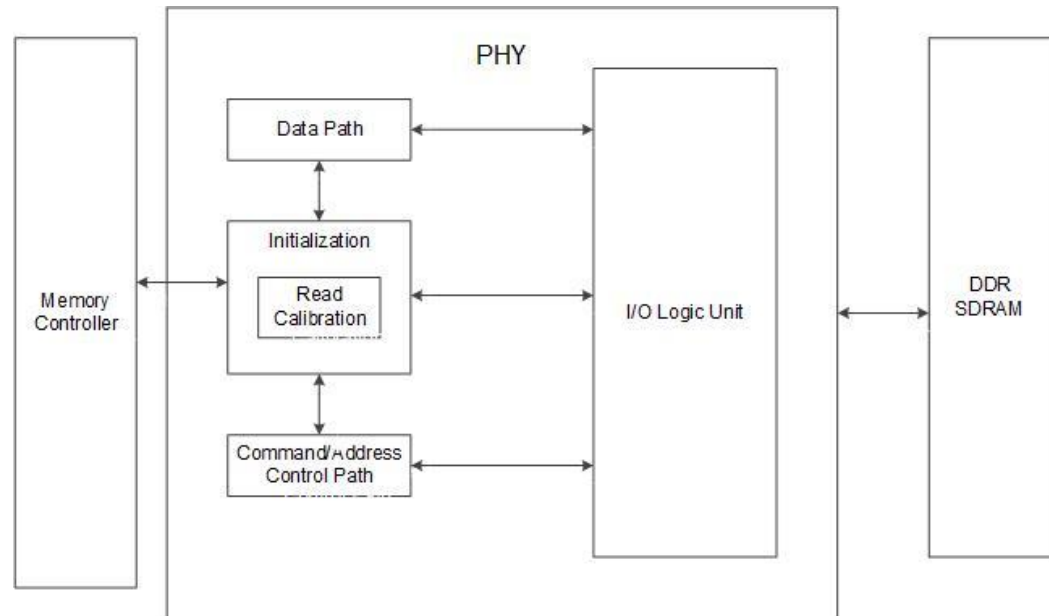
User-sent commands such as write and read are sequenced in Memory Controller to meet the data throughput rate and associated time parameter delays. Memory Controller controls delivering the address and data, and write or read through receiving the data from the DDR SDRAM using PHY.

3.3 PHY

The PHY provides the physical layer definition and interface between MC and external DDR SDRAM, receives commands from the MC memory controller, and provides DDR SDRAM interface with signals that meet the timing and sequence requirements.

The basic structure of PHY includes four modules: initialization module, data access, command address control path and I/O logic module, as shown in Figure 3-2.

Figure 3-2 DDR PHY Basic Structure



3.3.1 Initialization Unit

The initialization module mainly completes the initialization and read calibration of DDR SDRAM after power on. After all initialization and read calibration are finished, the signal "init_calib_complete" will be high to indicate the entire initialization completed.

Power-on Initialization

According to JESD79-F protocol standard, DDR SDRAM (chip or DIMM) is required to be initialized after power on, including the reset, clock enable, mode register configuration.

3.3.2 Data Path Unit

Data path unit includes the write data and read data.

3.3.3 Control Path Unit

Command/address control path is a single-pass, which receives the command and address signal sent by the MC, and cooperates with the data path, to process the write and read data time delay parameters and sends the commands to the I/O logic module.

3.3.4 I/O Logical Unit

Logic I/O module is mainly used to convert the clock domain of the data, command, and address signals received from the data path and command/address path.

3.4 Major Functions

The primary functions of Gowin DDR Memory Interface IP are as follows:

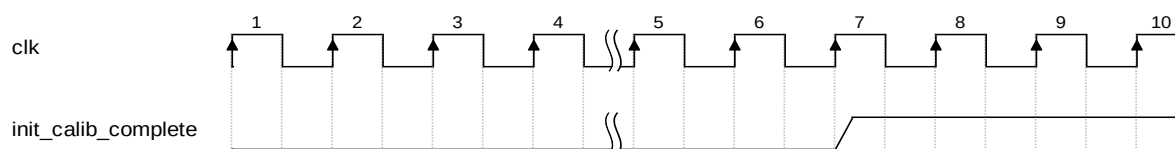
- Initialize DDR SDRAM
- Send the addresses and commands
- Write data
- Read data
- Refresh

3.4.1 Initialization

DDR SDRAM must be calibrated to perform write and read operations. Therefore, after power on, PHY will perform initialization calibration operation for DDR SDRAM; after the initialization is completed, the initialization completion flag `init_calib_complete` is returned.

The completion signal is returned to the user after initialization is completed, as shown in Figure 3-3.

Figure 3-3 Initialization Completed Signal Timing Diagram



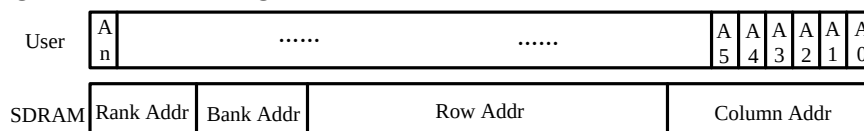
3.4.2 Send Addresses and Commands

You can send operation commands and addresses using the `addr`, `cmd`, and `cmd_en` interfaces.

- `Addr` is the address data interface;
- `CMD` is the command data interface;
- `Cmd_en` is the enable signal of the address and command, active high.

In the application, a mapping relationship exists between the address bus of a user interface and the physical memory Rank, Bank, Row, Column. In this design, the array is in Rank-Bank-Row-Column order. The addressing scheme is as shown in Figure 3-4. Users should note the order of addresses provided in the application.

Figure 3-4 Addressing Scheme in Rank-Bank-Row-Column Order



The commands sent by users using the CMD interface are as shown in Table 3-1.

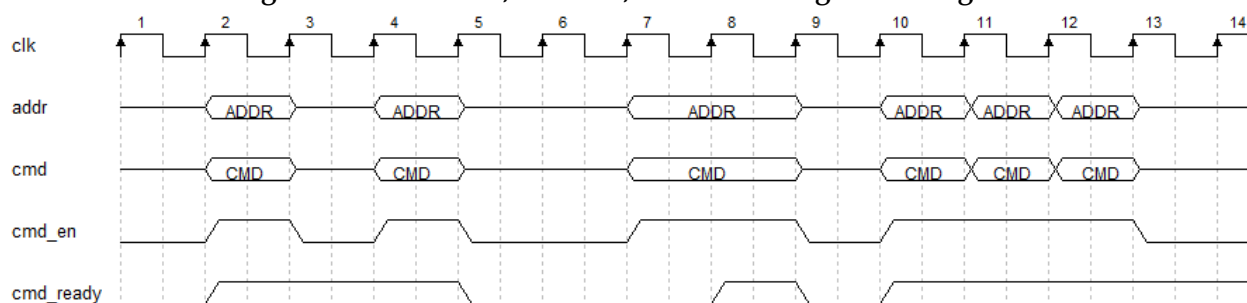
Table 3-1 cmd Command

Command	cmd[2:0]
Read	3'b001
Write	3'b000

At the user interface, the timing between the command, address, and the enabling signal are shown in Figure 3-5. The cmd_ready signal is at a high level, which indicates that the MC can receive the command, and the command can be saved in MC FIFO. If the cmd_ready signal is low, the MC cannot receive commands at this time.

When cmd_en is high, CMD and addr are active at this time. If cmd_en is changed to high when cmd_ready is low, cmd_en, cmd, and addr need to hold until cmd_ready is high so that the command can be saved in MC.

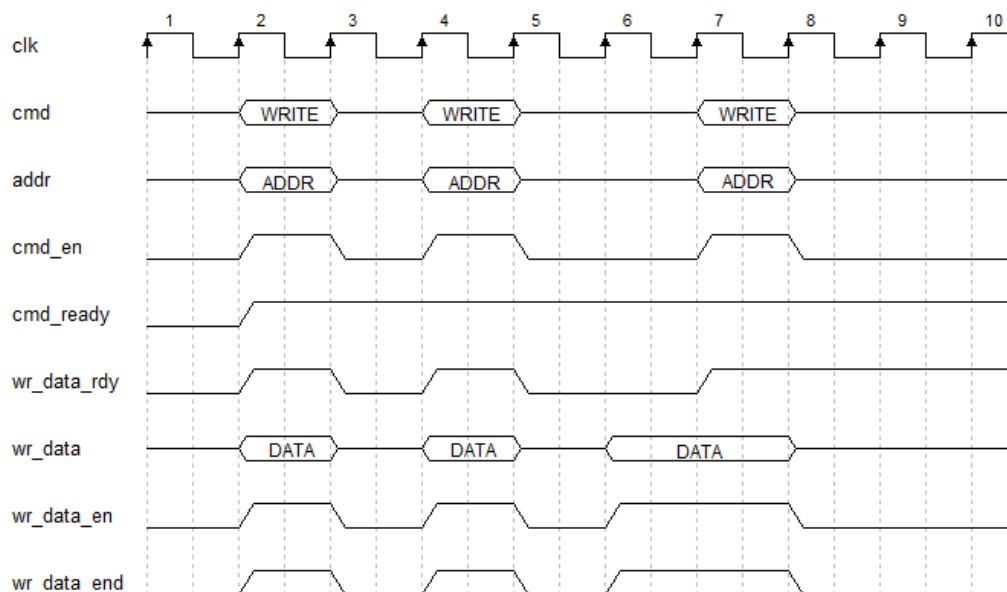
Figure 3-5 Command, Address, and Enable Signal Timing



3.4.3 Write Data

You can send write data to Gowin DDR Memory Interface IP through the user Interface wr_data, wr_data_wren, and wr_data_end, etc. The write data will be sent to DDR SDRAM after being processed.

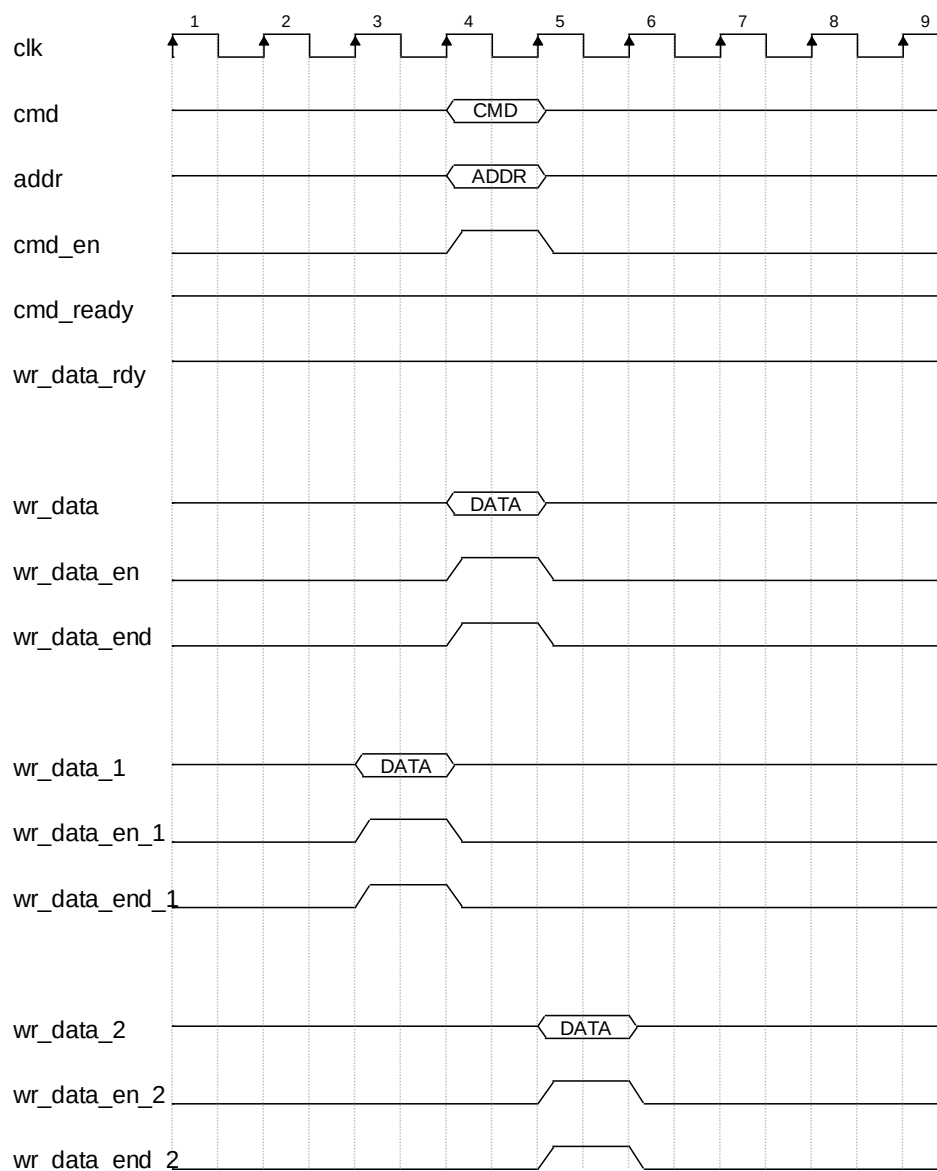
- Wr_data is a write data interface.
- Wr_data_en is a write data enable interface, write data is valid if it is high.
- Wr_data_end means occupying the last cycle required for writing this set of data in the current burst length.
- In the write data channel, the MC can receive the write data if wr_data_rdy is high.
- If the user sends the write data if wr_data_rdy is low. The wr_data, wr_data_en, and wr_data_end signals are maintained until wr_data_rdy is high, as shown in Figure 3-6.

Figure 3-6 Write Data Interface Timing

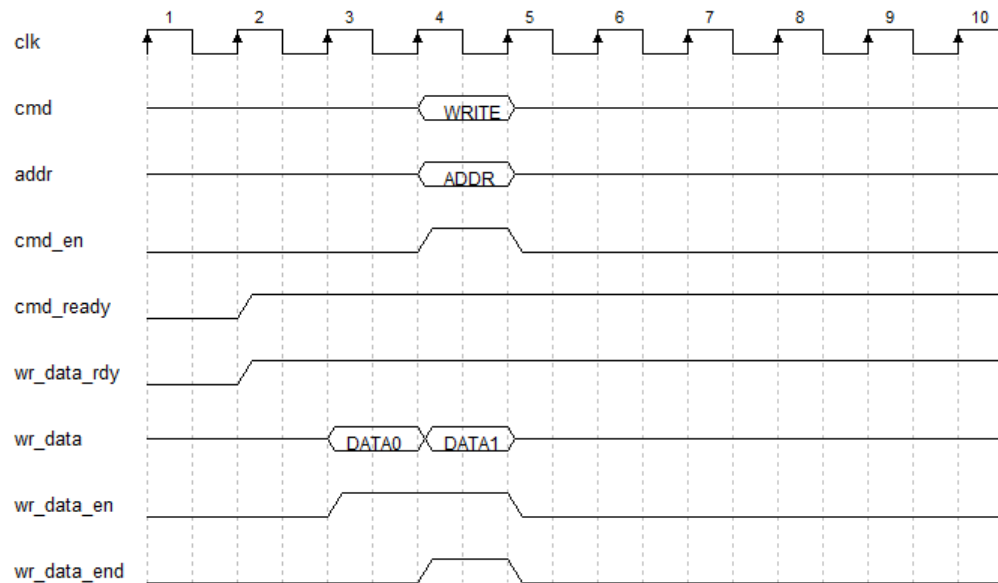
There are many timing situations between the data channel and the command channel, as shown in Figure 3-7:

- Send the write data and write commands simultaneously;
- Send the write data before the corresponding write commands;
- Send the write data after the corresponding write commands, but the delay period of the write data should be less than two cycles.

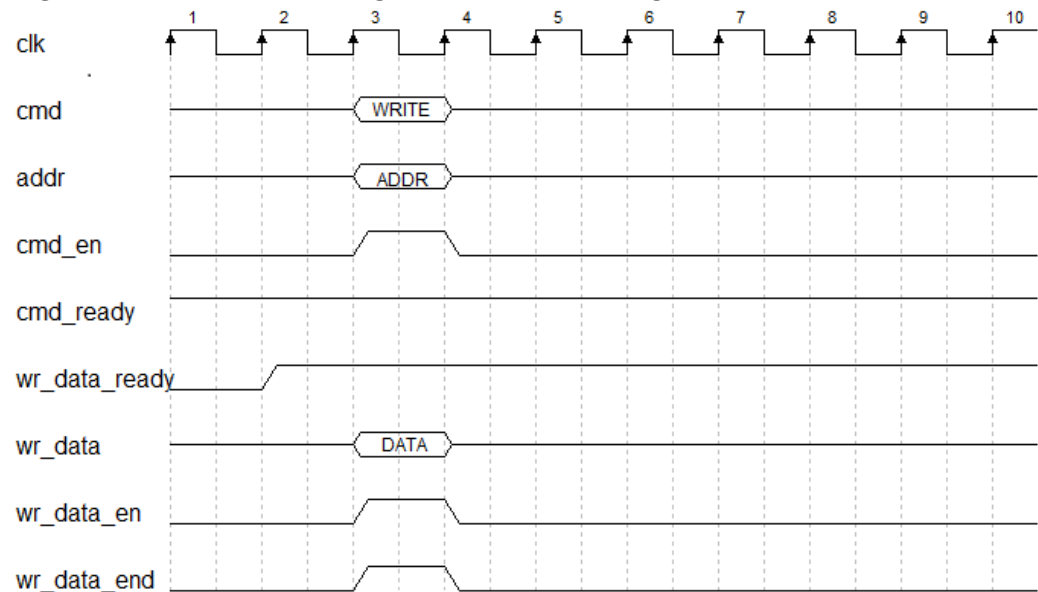
Figure 3-7 Write Data Channels and Command Channel Timing in Different Situations



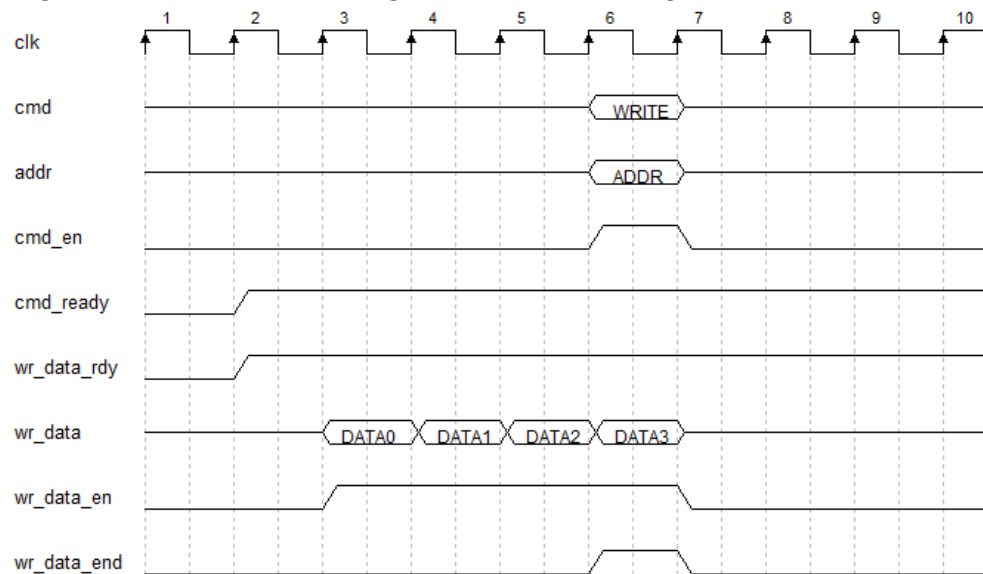
If the clock ratio of MC and PHY is 1:2, write data occupy two CLK cycles if the user configures a BL8 burst length, as shown in Figure 3-8. And the wr_data_end gets higher in the written data of the second period to indicate the write data to end.

Figure 3-8 Write Data Timing When the Burst Length is BL8

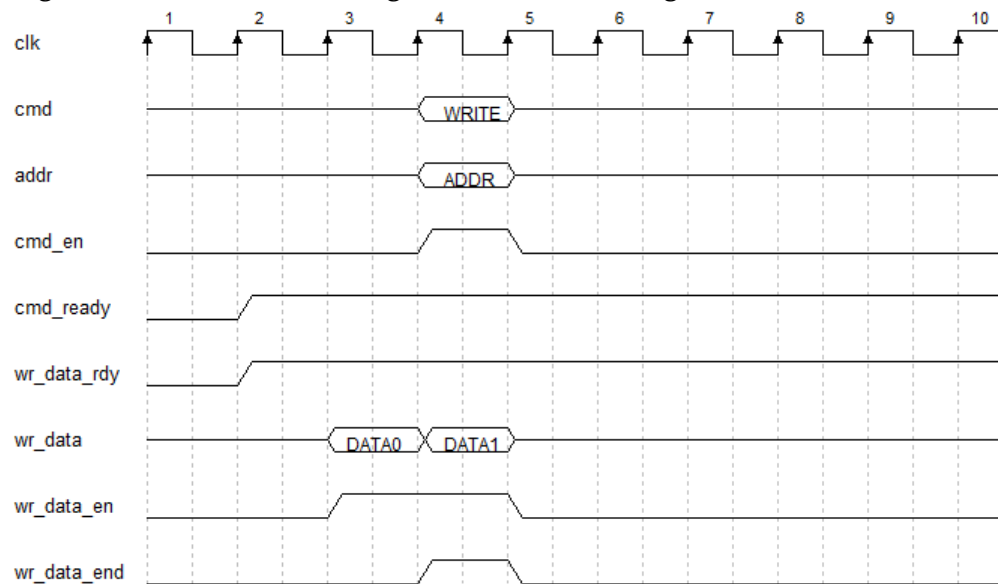
If the clock ratio of MC and PHY is 1:2, write data occupy one CLK cycle if the user configures a BL4 burst length, as shown in Figure 3-9.

Figure 3-9 Write Data Timing When the Burst Length is BL4

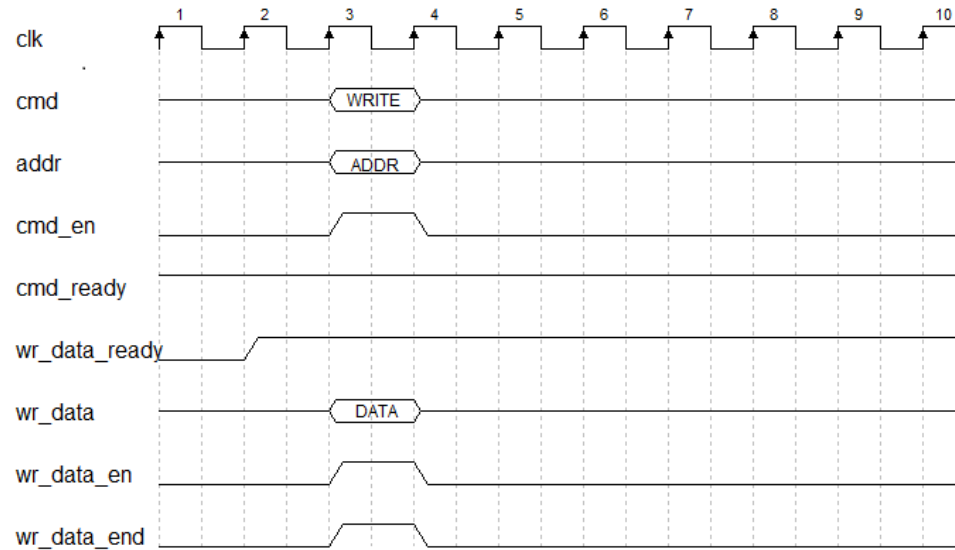
If the clock ratio of MC and PHY is 1:1, write data occupy four CLK cycles if the user configures a BL8 burst length, as shown in Figure 3-10. And the wr_data_end gets higher in the written data of the fourth period to indicate the write data to end.

Figure 3-10 Write Data Timing When the Burst Length is BL8

If the clock ratio of MC and PHY is 1:1, write data occupy two CLK cycles if the user configures a BL4 burst length, as shown in Figure 3-11. And the **wr_data_end** gets higher in the write data of the second period to indicate the write data to end.

Figure 3-11 Write Data Timing When the Burst Length is BL4

If the clock ratio of MC and PHY is 1:1, write data occupy one CLK cycle if the user configures a BL2 burst length, as shown in Figure 3-12.

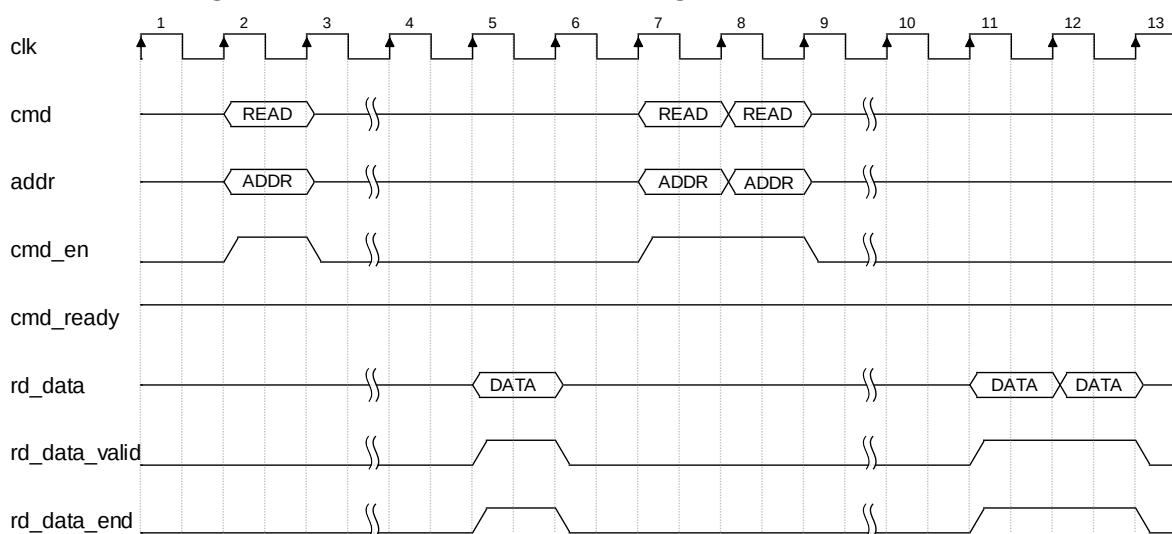
Figure 3-12 Write Data Timing When the Burst Length is BL2

3.4.4 Read data

You can read the data from DDR SDRAM using the user interfaces `rd_data`, `rd_data_valid`, and `rd_data_end`.

- The `rd_data` interface is the returned read data interface;
- The `rd_data_valid` interface signal is the valid read data interface. When it is high, the returned `rd_data` is valid at this time.
- The `rd_data_end` interface indicates the last set of returned data in the current burst length, and high power is usually valid.

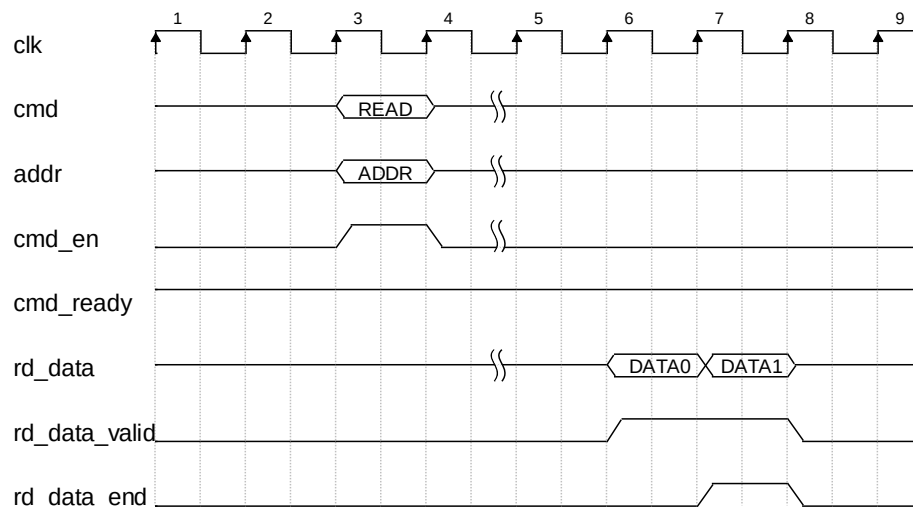
When the user reads multiple addresses continuously, the corresponding data will be returned in order of the address send to the read command.

Figure 3-13 Read Data Interface Timing

Similar to the write operation, if the clock ratio of MC and PHY is 1:2, read data occupy two CLK cycles if the user configures a BL8 burst length,

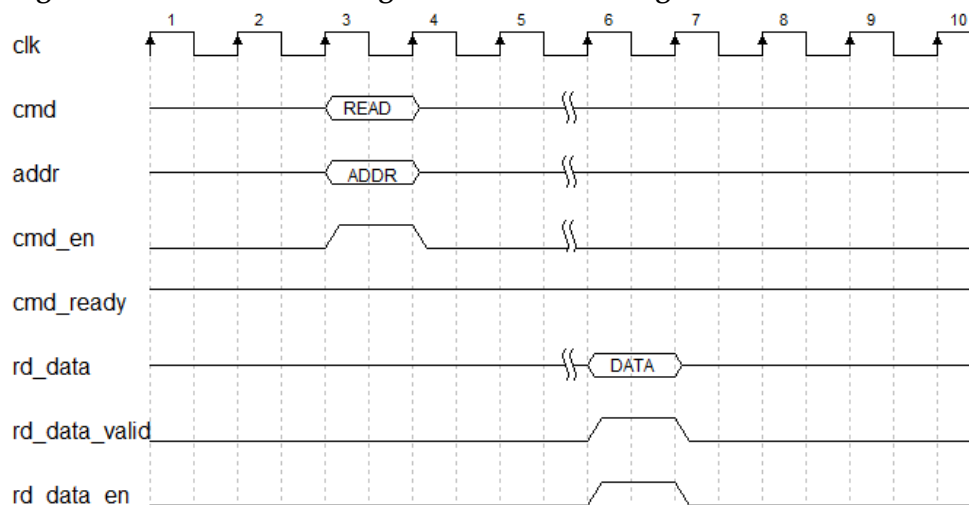
as shown in Figure 3-14.

Figure 3-14 Read Data Timing When the Burst Length is BL8

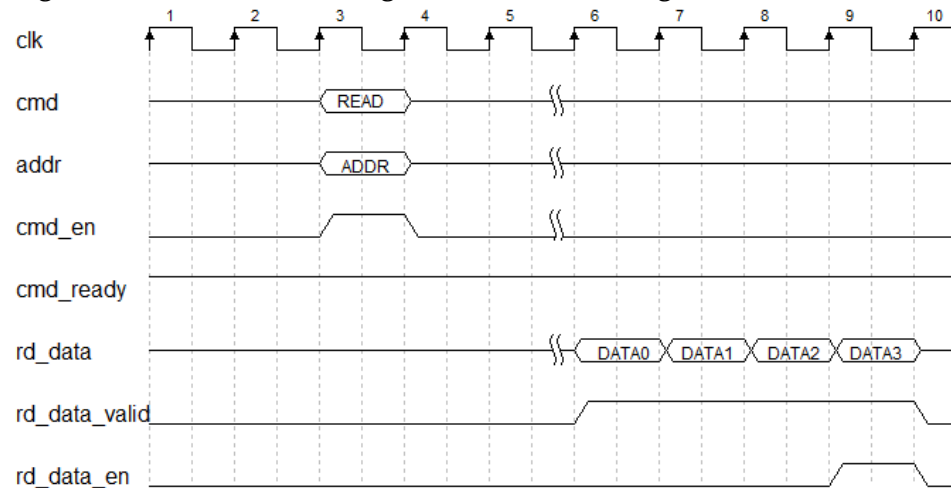


If the clock ratio of MC and PHY is 1:2, read data occupy two CLK cycles if the user configures a BL4 burst length, as shown in Figure 3-15.

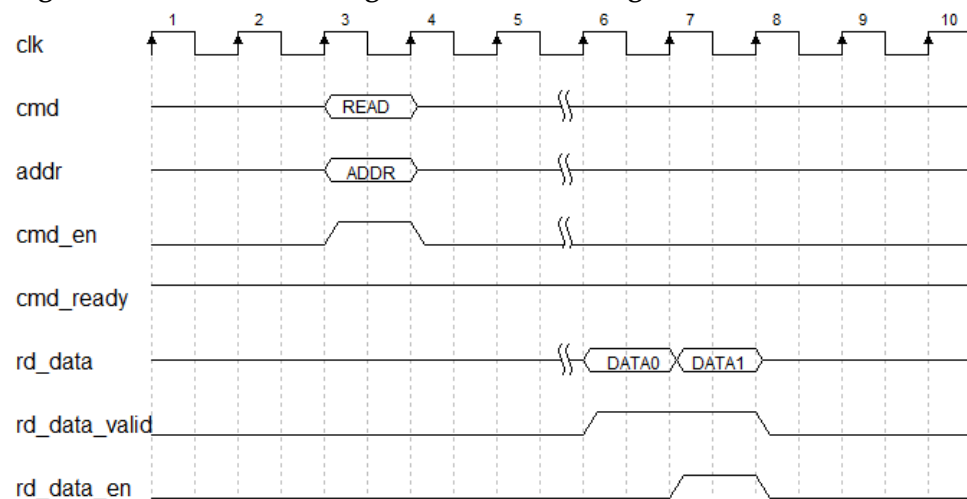
Figure 3-15 Read Data Timing When the Burst Length is BL4



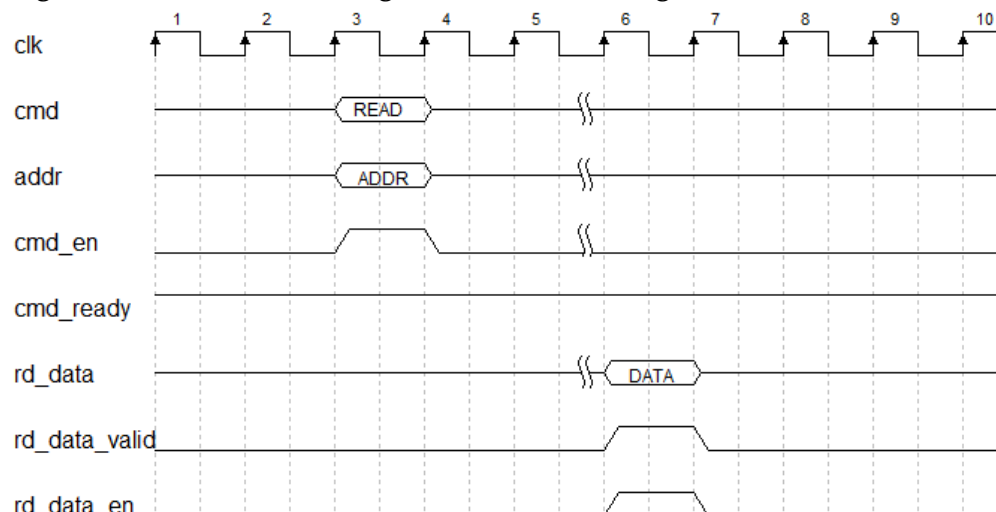
If the clock ratio of MC and PHY is 1:1, read data occupy two CLK cycles if the user configures a BL8 burst length, as shown in Figure 3-16.

Figure 3-16 Read Data Timing When the Burst Length is BL8

If the clock ratio of MC and PHY is 1:1, read data occupy one CLK cycle if the user configures a BL4 burst length, as shown in Figure 3-17.

Figure 3-17 Read data timing when the burst length is BL4

If the clock ratio of MC and PHY is 1:1, read data occupy two CLK cycles if the user configures a BL2 burst length, as shown in Figure 3-18 .

Figure 3-18 Read Data Timing When the Burst Length is BL2

3.4.5 Refresh

Refresh

DDR SDRAM memory array needs continually refresh to ensure that the data is not lost, so Gowin DDR Memory Interface IP is required to periodically send the refresh instructions to DDR SDRAM. Gowin DDR Memory Interface IP gaps the t_{REFI} time to generate refresh command. After executing the last one read and write command, MC will PreCharge all Banks, then execute the Refresh command. Refresh operation has the higher priority.

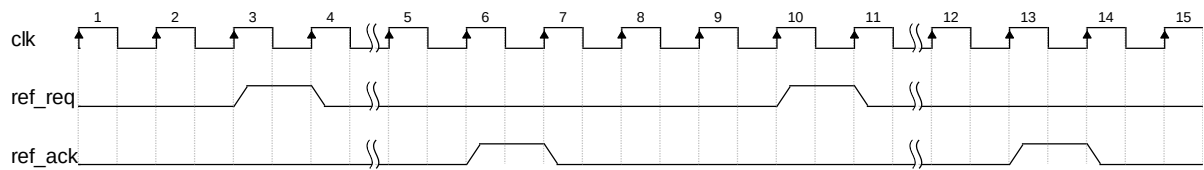
Self-Refresh

You can send a self-refresh request through the `sr_req` interface and configure DDR SDRAM to enter the self-refresh mode. In the self-refresh mode, DDR SDRAM will automatically refresh the memory array without the refresh instruction sent by Gowin DDR Memory Interface IP sends.

Gowin DDR Memory Interface IP will return the `sr_ack` signal to the user after completing the self-refreshing DDR SDRAM, indicating that the DDR SDRAM has entered the self-refresh mode.

User Refresh

You can use this option to configure the user refresh mode. "USER_REFRESH" needs to be set to "ON." You can refresh via the MC at any time using the `ref_req` interface without the requirement to send additional commands to the MC via the CMD interface. When sending the user refresh instruction, the `ref_req` is needed to continue a high level for one cycle. After sending the refresh instruction, the MC will feedback the `ref_ack` signal, and continue a high level for one cycle, as shown in Figure 3-19.

Figure 3-19 User Refresh Timing

The user refresh operation may affect the commands that the MC has received or is executing. Before operating the user refresh, the MC will execute the commands that are in the process of being executed. Users should consider the coordination between the user refresh and other instructions to avoid violating t_{REFI} .

In the worst-case scenario, you can refer to following formula and specify a certain time to complete the transfer by roughly calculating the t_{RCD} , CL, data transmission time, t_{RP} etc., and completing the user refresh before the time parameter t_{REFI} violated; so the maximum interval between two user refresh times is approximately:

$$t_{REFI} - (t_{RCD} + (CL + 4) \times t_{CK} + t_{RP}) \times nBA$$

In the actual application, if the user refresh starts, the user will need to send a refresh command immediately after finishing the DDR SDRAM initialization. This will establish the time benchmark for subsequent users to refresh the request.

4 Port List

The I/O ports of Gowin DDR Memory Interface IP are shown in Table 4-1.

Table 4-1 IO Port of Gowin DDR Memory Interface IP

Signal	Data Width	I/O	Description
User Interface			
addr	ADDR_WIDTH	Input	Address input; the width is configurable through a parameter.
cmd	3	Input	Command channel
cmd_en	1	Input	Command and address enable signals: 0: invalid 1: valid
cmd_ready	1	Output	Indicates the Memory Interface is ready to accept commands and addresses when high.
rd_data	APP_DATA_WIDTH	Output	Read data channel
rd_data_end	1	Output	High indicates the last cycle of the current rd_data group.
rd_data_valid	1	Output	rd_data valid signal: 0: invalid 1: valid
burst	1	Input	Reserved, fixed to 0.
wr_data	APP_DATA_WIDTH	Input	Write data channel
wr_data_end	1	Input	High indicates the last cycle of the current wr_data group.
wr_data_mask	APP_MASK_WIDTH	Input	Mask signal for wr_data
wr_data_rdy	1	Output	High indicates the MC can accept user write data.
wr_data_en	1	Input	wr_data enable signal: 0: invalid 1: valid
sr_req	1	Input	Self refresh request
sr_ack	1	Output	Refresh the acknowledgement signal
ref_req	1	Input	User refresh request

Signal	Data Width	I/O	Description
ref_ack	1	Output	User refresh acknowledge
clk	1	Input	Reference input clock
memory_clk	1	Input	Chip operating clock, typically a high-speed PLL-multiplied clock.
pll_lock	1	Input	Connect to PLL pll_lock when memory_clk uses a PLL; tie to 1'b1 if the PLL is not used.
rst_n	1	Input	Reset input, active low.
init_calib_complete	1	Output	Initialization completed signal
clk_out	1	Output	User design clock, running at either 1/2 or 1/1 of the Memory Clock frequency
ecc_err	APP_DATA_WIDTH/ 32	Output	ECC status indication output signal
ddr_rst	1	Output	Reset signal processed by the IP, provided for the user logic, active-high
dbg_vector1_out	3*DQS_WIDTH	Output	Debug port, used only when debug port is enabled
dbg_vector2_out	2*DQS_WIDTH	Output	Debug port, used only when debug port is enabled
dbg_vector3_out	8	Output	Debug port, used only when debug port is enabled
DDR SDRAM Interface			
O_ddr_addr	ROW_WIDTH	Output	Row address (activation command), Column address (read/write command)
O_ddr_ba	BANK_WIDTH	Output	Bank address
O_ddr_cs_n	CS_WIDTH	Output	Chip selected, active-low.
O_ddr_ras_n	1	Output	Row address strobe signal
O_ddr_cas_n	1	Output	Column address strobe signal
O_ddr_we_n	1	Output	Row write enable
O_ddr_ck	CK_WIDTH	Output	A clock signal provided for DDR SDRAM
O_ddr_ck_n	CK_WIDTH	Output	Composes a differential signal with ddr_ck
O_ddr_cke	CKE_WIDTH	Output	DDR SDRAM clock enable signal
O_ddr_reset_n	1	Output	DDR SDRAM reset signal
O_ddr_dqm	DM_WIDTH	Output	DDR SDRAM data masking signal
IO_ddr_dq	DQ_WIDTH	Bidirection	DDR SDRAM data
IO_ddr_dqs	DQS_WIDTH	Bidirection	DDR SDRAM data strobe signal. When selecting devices from the LittleBee family and performing schematic design, you must ensure that when assigning the ddr_dqs pin, one differential pair (A and B) is left unconnected, and the adjacent differential pair with the next lower pin numbers is also left unconnected. For example, if ddr_dqs is assigned to IOB16A, then IOB16B, IOB15A, and IOB15B must all be left unconnected.

5 Parameter Configuration

Gowin DDR Memory Interface IP supports DDR SDRAM devices. You need to configure a variety of static parameters and timing parameters of Gowin DDR Memory Interface according to the design requirements, as shown in Table 5-1 and Table 5-2.

Table 5-1 Static Parameter Options of Gowin DDR Memory Interface

Name	Description	Options
DRAM_TYPE	Memory type	DDR
DRAM_WIDTH	DQ Width of DDR chip	4, 8, 16
ADDR_CMD_MODE	Address command mode	1T, 2T
nCK_PER_CLK	Clock ratio between MC and PHY interfaces	1:1/1:2 (LittleBee Family supports only the 1:2 option)
nCS_PER_RANK	The number of each Rank CS	1
APP_ADDR_WIDTH	Address Width	RANK_WIDTH + BANK_WIDTH + ROW_WIDTH + COL_WIDTH
BANK_WIDTH	Memory BANK address width	Select according to DDR SDRAM chip
CS_WIDTH	CS bit width	Select according to DDR SDRAM chip
RANK_WIDTH	BANK address width	Select 1 for single and dual rank devices;
ROW_WIDTH	DRAM ROW address width	Select according to DDR SDRAM chip
DM_WIDTH	Data mask bit width	DQ_WIDTH/ DRAM_WIDTH
DQ_WIDTH	DQ signal width	DQ_WIDTH=DRAM_WIDTH * DQS_WIDTH
DQS_WIDTH	DQS signal width	DQ_WIDTH/8
BURST_MODE	Burst length	"2", "4", "8" (LittleBee Family supports only "4" and "8")
BURST_TYPE	Read and write data when bursting	"Sequential" "Interleaved"
RTT_NOM	Nominal ODT value	"150": 150

Name	Description	Options
		"75": 75 "50": 50
RTT_WR	The Dynamic ODT value in Multiple-RANK used for the write interface is invalid for RTT_WR of Single-Component Design;	"OFF": RTT_WR disabled. "120": RZQ/2 "60": RZQ/4
APP_DATA_WIDTH	Data signal width at the user interface	$APP_DATA_WIDTH = 2 * nCK_PER_CLK * DQ_WIDTH$
APP_MASK_WIDTH	Mask signal width at the user Interface	$APP_DATA_WIDTH/DRAM_WIDTH$
USER_REFRESH	Whether to control the refresh operation by the user	"ON", "OFF"
DBG_PARAMETER1	Debug parameter	000/001/010/011/100/101/110/111, used only when debug parameter is enabled.
DBG_PARAMETER2	Debug parameter	0~127, used only when debug parameter is enabled.
DBG_PARAMETER3	Debug parameter	0~127, used only when debug parameter is enabled.
DBG_PARAMETER4	Debug parameter	0~127, used only when debug parameter is enabled.

Table 5-2 DDR Time Parameter

Name	Description
t _{CK}	Memory interface clock period (ps)
t _{CKE}	Minimum pulse time of CKE signal (ps)
t _{FAW}	In the same rank, it can concurrently send the interval time that is more than four rows of active commands, so the minimum value should be more than four times t _{RRD} .
t _{RAS}	Time from ACTIVE to PRECHARGE
t _{RCD}	Time from ACTIVE to READ / WRITE
t _{REFI}	Memory refresh interval
t _{RFC}	The interval from REFRESH to ACTIVE / REFRESH
t _{RP}	PRECHARGE cycle
t _{RRD}	The interval from ACTIVE to ACTIVE
t _{RTP}	The interval from READ to PRECHARGE
t _{WTR}	The interval from WRITE to READ
AL	Additive latency
CL	CAS latency
WR_CYC	Write recovery for auto precharge

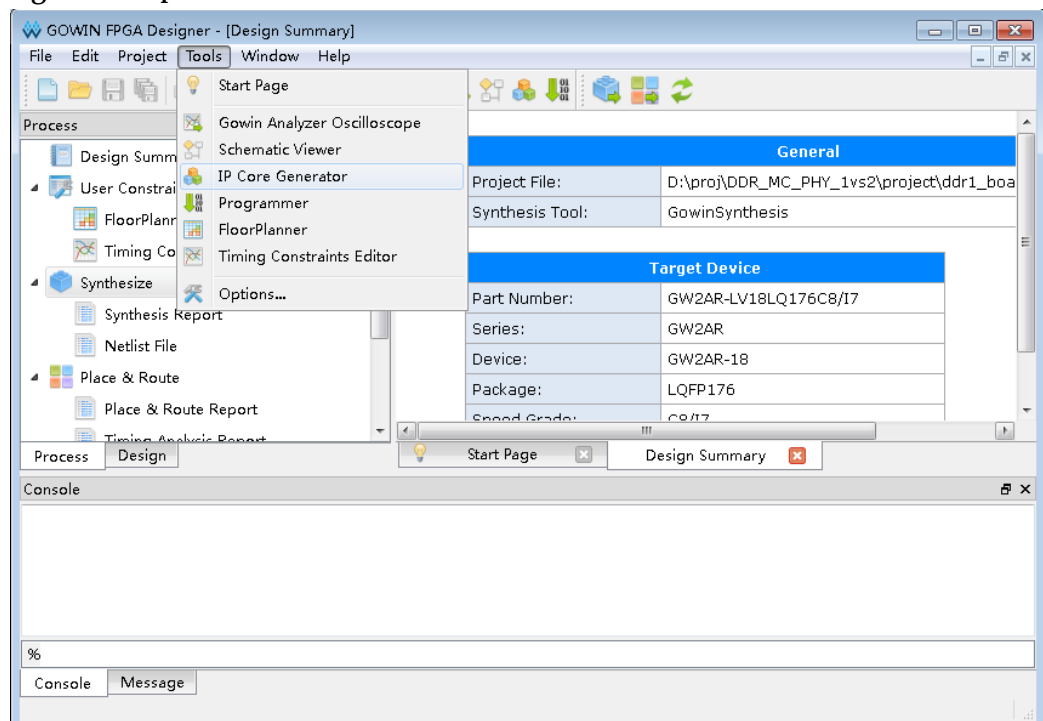
6 Interface Configuration

You can invoke and configure Gowin DDR Memory Interface IP through the IP Core Generator tool in the IDE. In this chapter, take EM6A9160-4 memory as an example, introduce the main configuration interface, configuration flow and the meaning of each configuration option.

1. Open the IP Core Generator

After creating the project, you can click the Tools tab in the upper left and select the IP Core Generator via drop-down to open the Gowin IP Core Generator, as shown in Figure 6-1.

Figure 6-1 Open IP Core Generator

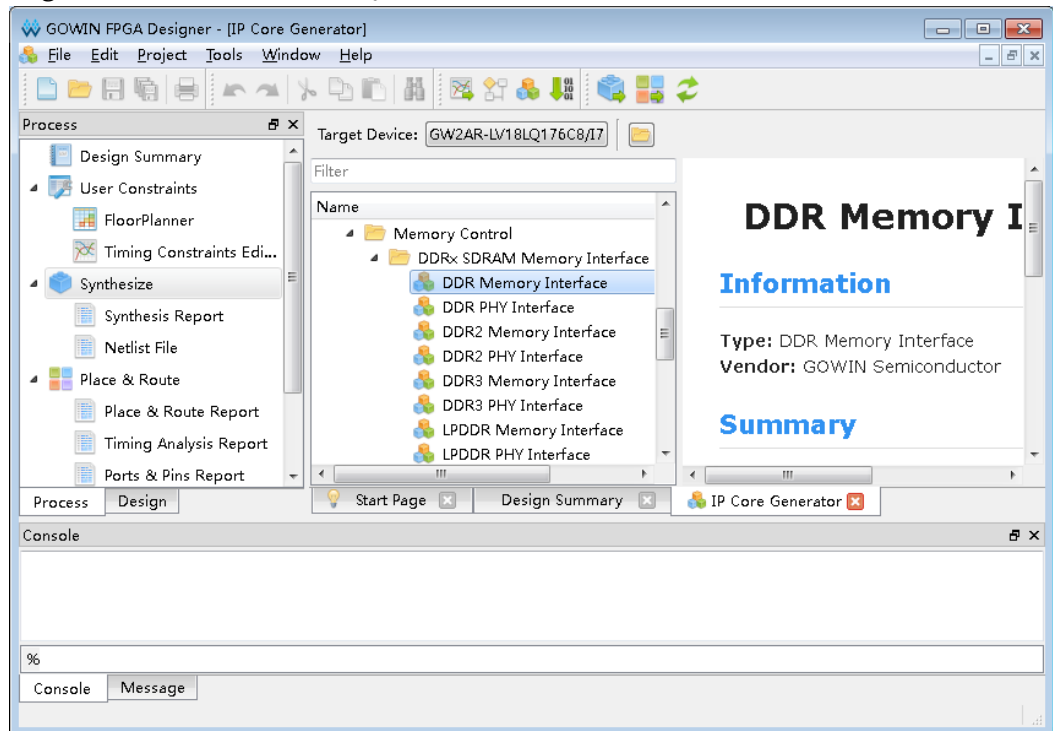


2. Open DDR Memory Interface IP core

Click the "DDRx SDRAM Memory Interface" option, double-click DDR Memory Interface. DDR Memory Interface IP core opens, as shown

in Figure 6-2.

Figure 6-2 Open DDR Memory Interface IP core

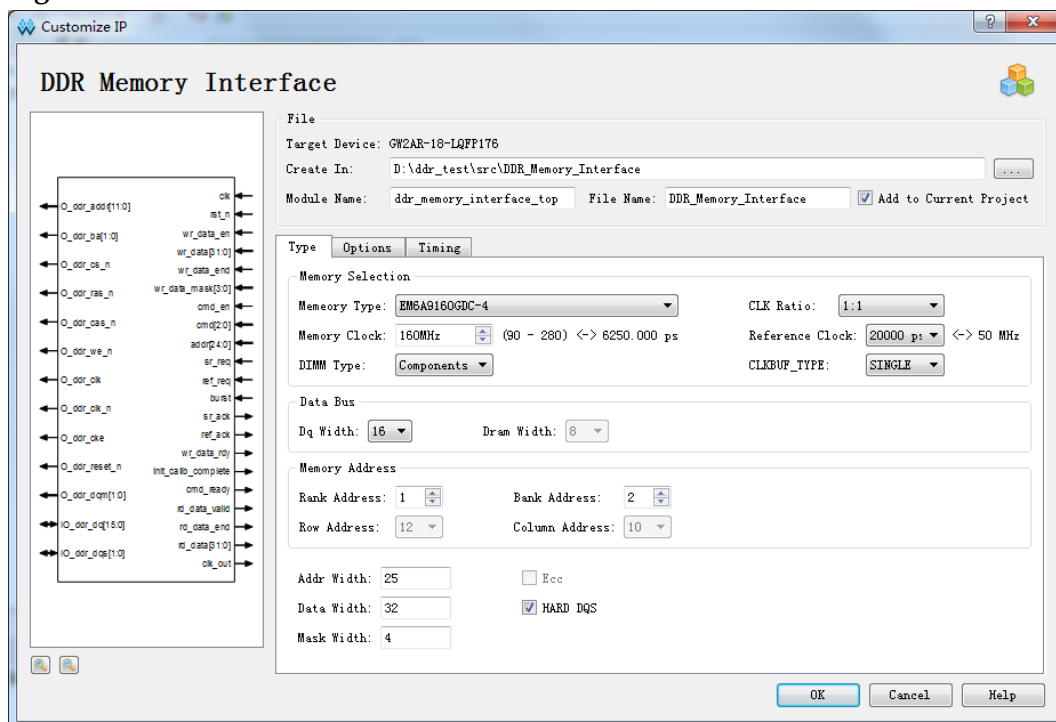


3. DDR Memory Interface IP Core Interface

The Interface view of DDR Memory Interface IP core is on the left, as shown in Figure 6-3.

The left end is the interface between DDR Memory Controller and the user port. You can connect your design to DDR Memory Interface IP to send/receive commands and data. The right end is the interface between the physical interface (PHY) and the memory chip. You can access data through connecting DDR Memory Interface IP core and the memory chip. With different configuration information, the signal bit-width and the signal number will change accordingly.

Figure 6-3 IP Core Interface View

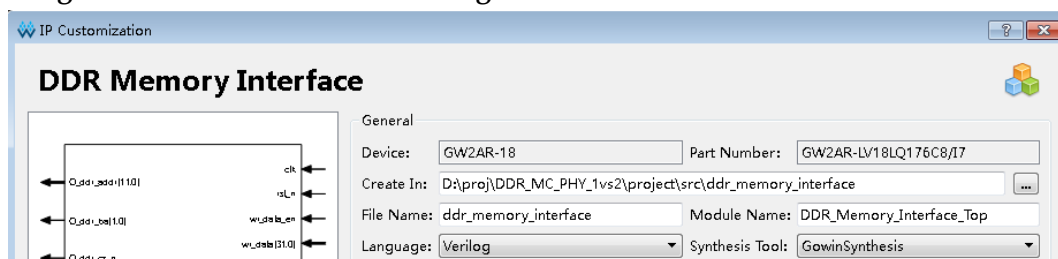


4. Configure Basic Information

See the basic information in the upper part of the configuration interface. Take the GW2AR-18 chip as an example, and select the package LQFP-176.

- "Module Name" is the top-level file name after the project is generated. "DDR_Memory_Interface_Top" by default, you can modify the name.
- "File Name" is the folder generated by the IP core file, which is used for saving the files of DDR Memory Interface IP core, "ddr_memory_interface" by default. You can modify the name.
- "Create In" is the path generated by the IP core folder. "\project path src\ddr_memory_interface" by default. You can modify the path.

Figure 6-4 Basic Information Configuration Interface



5. Type Options

In the Type Options, you need to configure the basic information for DDR memory chip, as shown in Figure 6-5.

- Select Memory Options

- In Memory Type options, the memory model is firstly chose. Take EM6A9160-4 memory as an example, the relevant parameters based on the memory model will generate by default after selecting the memory model. You can also modify it as required. If you select the Custom option, the related parameters are needed to modify and generate manually.
- The CLK Ratio option is the clock Ratio of the GOWIN memory controller and physical interface, which only supports 1:1/1:2 temporarily. The user can select.
- The Memory Clock is the clock frequency of Gowin Memory controller. You can arbitrarily choice the clock frequency between 90~250MHz, the options will be automatically converted to cycle, unit ps, 160MHz (i.e. 6250ps) by default, the data rate is 2 times more than the Memory Clock.
- For DIMM Type, you can select RDIMMS, UDIMMS, SoDIMMS, and Componets.
- Data Bus Options
 - Dq Width is the data bit-wide of the memory. You can choose 8, 16, 24, 32, 40, 48, 56, 64, 72. When choosing 72, can optionally check the ECC option, otherwise ECC is not allowed to choic.
 - Dram Width is DQ Width of DDR chip, you can not modify after DDR memory is determined. If the Custom is selected in the Memory Type, you can fill in it.
- Memory Address Options

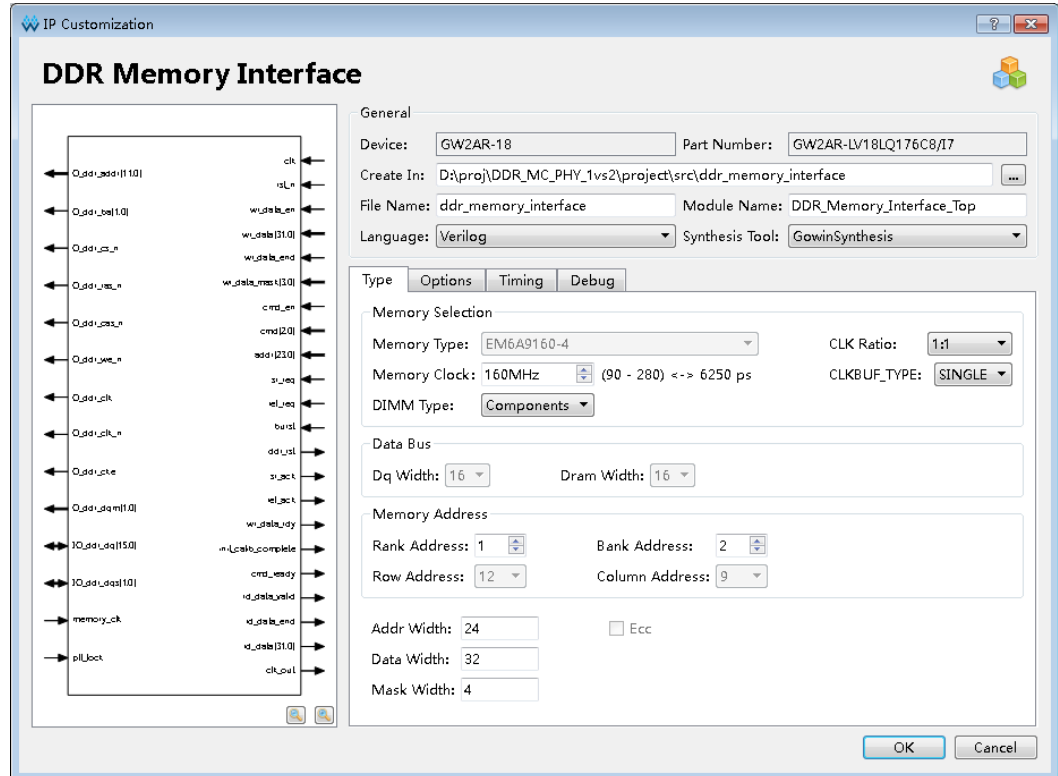
In Memory Address, you can mainly fill in the Address information of the Rank, Bank, Row and Column of DDR memory. After choosing the DDR memory type, GUI will be automatically fill in; if you choose the Custom, you need to optionally choose according to the DDR Memory type.
- ECC Option

Checked only when the user selects a 72 DQ width, i.e., 64 data DQ width, and the other 8 DQ widths are the ECC check widths.

Note!

The Width of Addr Width is Rank+Bank+Row+ Colum; Data Width is 4* Dq (clock ratio is 1:2) or 2*DQ (clock ratio is 1:1); Mask Width is Data Width/Dram Width. The above three options are calculated by Gowin Software, and you cannot operate.

Figure 6-5 Type Options



6. Options

● Memory options

- Burst Mode is used for selecting the Burst length, which can choose 2, 4 or 8, 4 by default (2 is not optional if clock ratio is 1:2).
- Burst Type is an emergency Type selection, which can be Sequential or Interleaved, SEQ by default.
- User Refresh is used to ask whether to open the refresh request the user sent, the default is unchecked, self-refresh controlled by the GOWIN Memory Controller.

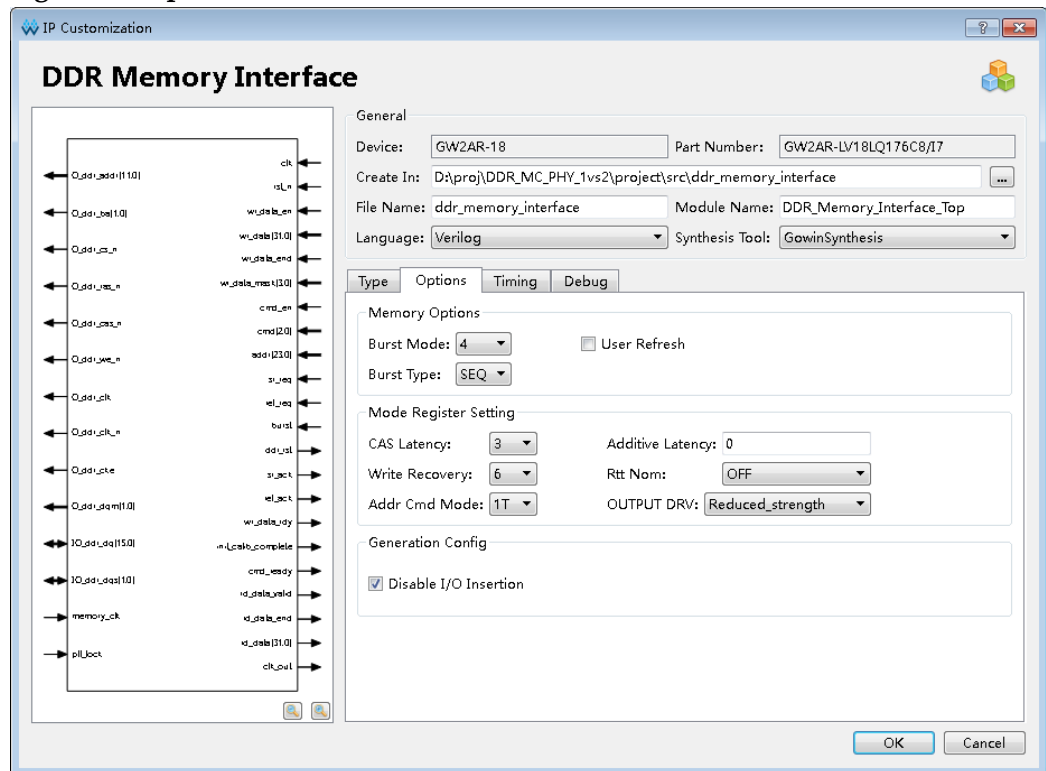
● Mode Register Setting

- CAS Latency is the CL parameter in DDR memory, i.e., the selection and Latency period of the column address pulse. 4 by default. You can select the option 2/2.5/3 as required;
- Additive Latency is the AL parameter in DDR memory, i.e., the additional time delay. 0 by default. You can select the option 0 as required;
- Write Recovery is the WR parameter of DDR memory, 6 by default. You can select the option 2/3/4/5/6 as required;
- Rtt Nom is the ODT resistance parameter of DDR memory, OFF by default. You can select the option OFF/ 75/150/50 as required;
- Add Cmd Mode is the command time type of the DDR memory, the default is 1T. You can select the option 1T/ 2T as required;

- OUTPUT DRV is the OUTPUT driver option in DDR memory, Full strength by default, you can select the option Full strength/Reduce strength as required.
- Generation Config Options

If it is checked, IBUF, OBUF and other primitives are not inserted in the generated IP; and the logic is directly connected using the port, the default is checked.

Figure 6-6 Options



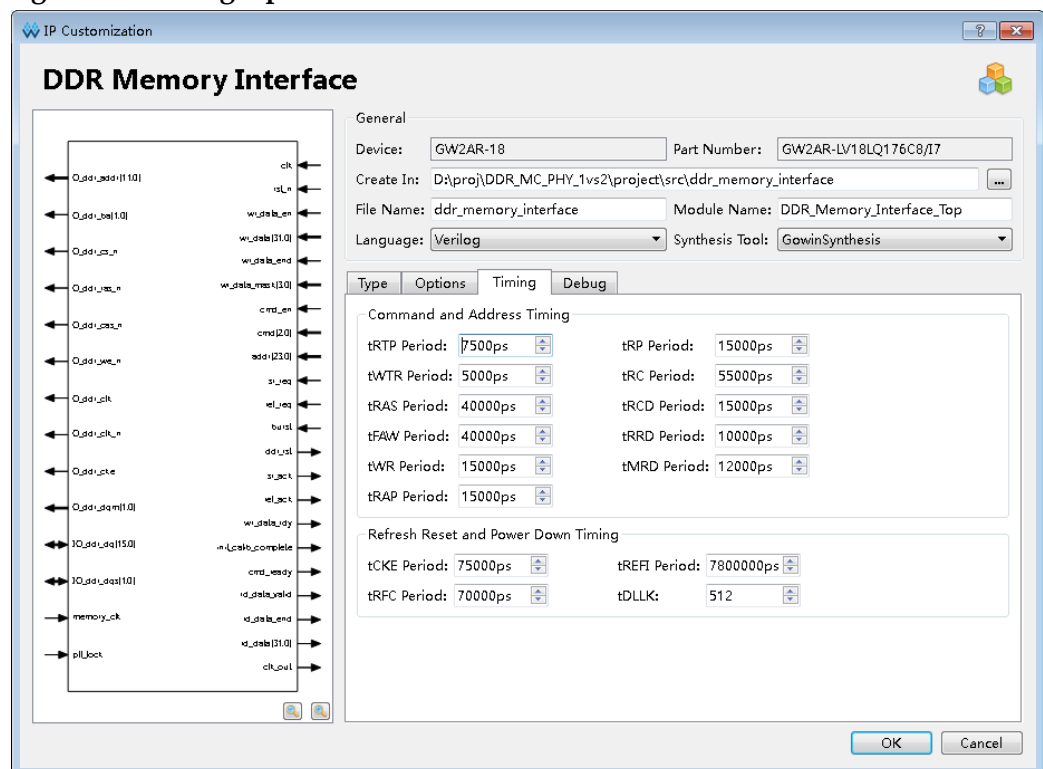
7. Timing Options

- Command and Address Timing Options
 - tRTP Period is the time interval between READ to PRECHARGE in DDR memory, 7500ps by default. You can modify it.
 - tRP Period is the PRECHARGE cycle in DDR memory, 12500ps by default. You can modify it.
 - tWTR Period is the time interval between WRITE to READ in DDR memory, 75000ps by default. You can modify it.
 - tRC Period is the time delay between ACTIVE to ACTIVE in DDR memory, 55000ps by default. You can modify it.
 - tRAS Period is the time in DDR memory from ACTIVE to PRECHARGE, 37500 by default. You can modify it.
 - tRCD Period is the time in DDR memory from ACTIVE to READ/WRITE, 12500 by default. You can modify it.
 - tFAW Period is the time interval in the same rank of DDR memory

which is allowed to concurrently send more than four rows of active commands, so the min. value should be more than four times of tRRD. 40000ps by default. You can modify it.

- tRRD Period is the min. interval between ACTIVE to ACTIVE in DDR memory, 7500ps by default. You can modify it.
- tWR Period, write recovery time.
- tMRD Period, mode register set cycle time.
- tRAP Period, activate to automatic precharge delay.
- Refresh, Reset and Power Timing options
 - tCKE Period is the min. pulse time (ps) of the CKE signal in DDR memory, 75000ps is by default. You can modify it.
 - tREFI Period is the refresh time interval of DDR memory, 7800000ps by default. You can modify it.
 - tRFC Period is the interval from REFRESH to ACTIVE/REFRESH in DDR memory, 160000ps by default. You can modify it.
 - tDLLK Period is the DLL cycle No., 512 by default. You can modify it.

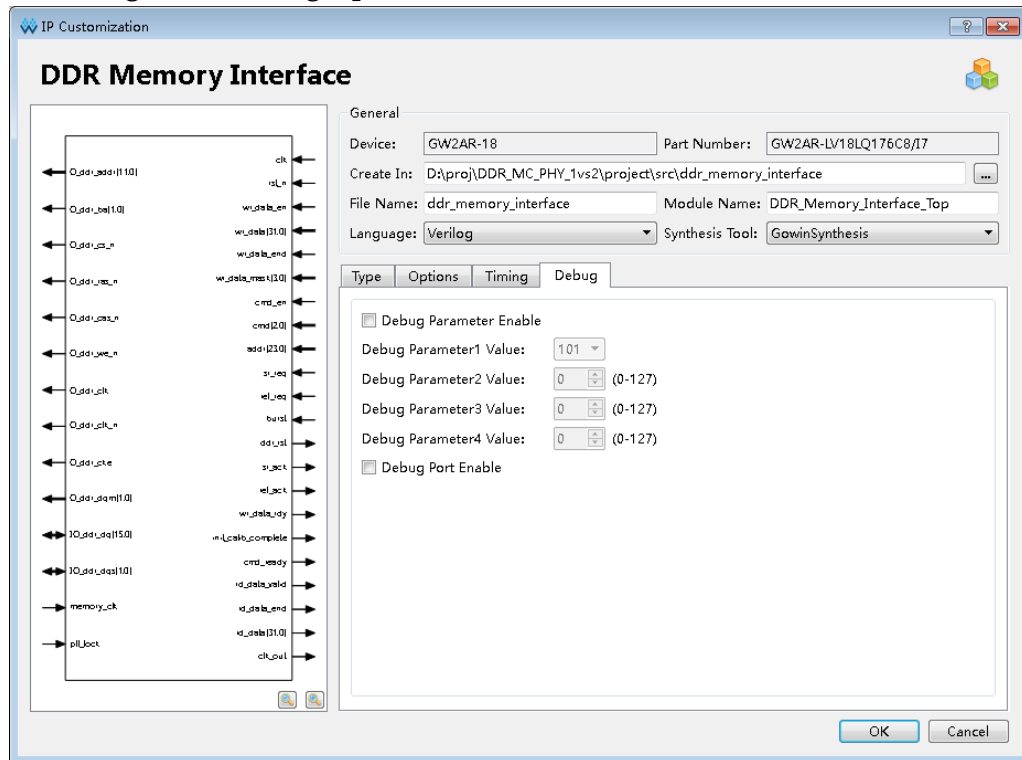
Figure 6-7 Timing Option



8. Debug Options

Debug option is as shown in Figure 6-8. Check it to open the debug parameters and debug port, and you can contact Gowin FAE to learn the meanings of the corresponding parameters and ports.

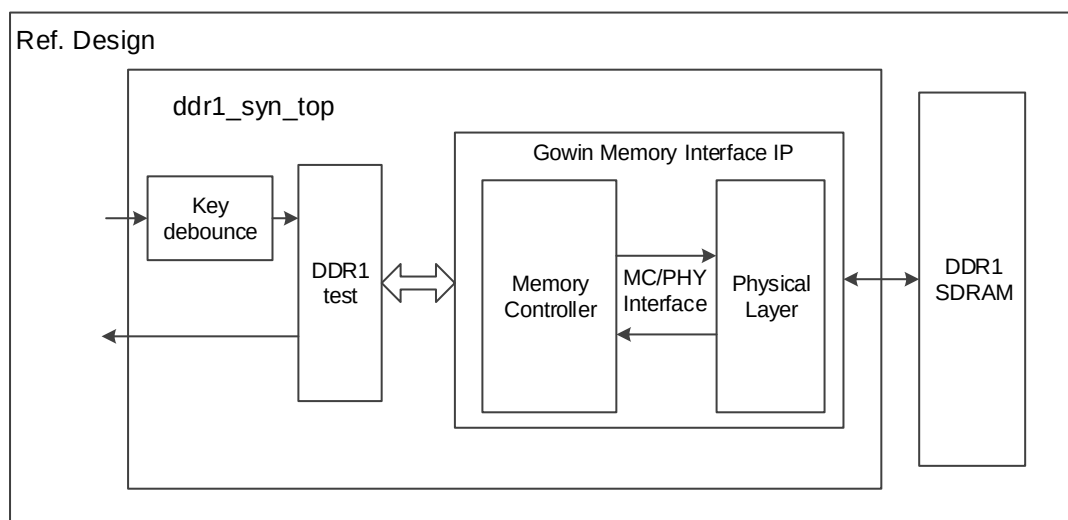
Figure 6-8 Debug Options



7 Reference Design

To quickly learn and use Gowin DDR Memory Interface IP, a simple [reference design](#) is provided for the users. The basic structure of reference is shown in Figure 7-1.

Figure 7-1 Basic Structure of Reference Design



In the reference design, ddr1_syn_top module is the top-level module unit and its interfaces are connected to the input reference clocks, external reset signals, etc. The interface connection is as shown in Table 7-1. DDR1_test is used to generate address, data and read/write commands required by Gowin Memory Interface IP, and the module can be synthesized.

Table 7-1 ddr_syn_top Module Input Interface List

Name	Description
clk	Input reference clock, 50MHz by default
rst_n	Input reset signal

The DDR1_test performs write and read operations for different addresses. You can modify the written address and data, etc., analyze and

8 File Delivery

The delivery file for Gowin DDR Memory Interface IP includes document, design source code, and reference design.

8.1 File

The folder mainly contains PDF files for the user guide.

Table 8-1 File List

Name	Description
IPUG507, Gowin DDR Memory Interface IP User Guide	Gowin DDR Memory Interface IP User Guide

8.2 Design Source Code (Encryption)

The Encryption Code Folder contains the RTL encryption code of Gowin DDR Memory Interface IP used for the GUI, to concertedly generate the IP cores as needed.

Table 8-2 Design Source Code List

Name	Description
DDR_TOP.v	The top-level files of IP core, which provide users with interface information, unencrypted.
ddr_name.v	Project naming files, the project names are imported from the GUI, unencrypted.
gwmc_param.v	Gowin memory controller parameter configuration module, which is generated by the user via the GUI, unencrypted.
gwmc_local_param.v	Gowin memory controller parameter processing module, which disposes the parameters passed from the GUI, encrypted.
ddr_code.v	Encryption code

8.3 Reference Design

The Ref.design folder contains the netlist file for Gowin DDR Memory Interface IP, the user reference design, the constraint file, the top file, and the project files.

Table 8-3 Ref.Design Folder Contents List

Name	Description
ddr1_syn_top.v	The top module of reference design
DDR1_test_rst.v	Test stimulus generation module
DDR_Memory_Interface.vo	Gowin DDR Memory Interface IP netlist file
ddr.cst	Physical Constraints File
ddr.sdc	Physical Constraints File
DDR_Memory_Interface	DDR IP folder

