GW1N series of FPGA Products

Data Sheet

DS100-3.3.4E, 11/13/2026

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Revision History

Date	Version	Description
03/31/2016	1.05E	Initial version published.
07/31/2018	1.2E	● PLL Structure diagram updated. ● User Flash timing parameters added. ● Description of GPIO status for blank chips added.
09/08/2018	1.3E	The UG256 package added.
11/27/2018	1.4E	● B version devices added. ● Bank0 and Bank2 of GW1N-6 and GW1N-9 support I3C OpenDrain/PushPull conversion. ● The step delay of IODELAY changed from 25ps to 30 ps.
01/09/2019	1.5E	Oscillator frequency updated.
02/14/2019	1.6E	● Power supplies for UV devices updated; ● Recommended Operating Conditions for UV devices updated. ● Part naming figures updated.
06/04/2019	1.7E	● Operating temperature changed to Junction temperature. ● GW1N-1S added. ● Power supply restrictions of Bank0/1/3 in GW1N-6/9 added. ● Description of User Flash in GW1N-2/2B/4/4B/6/9 added.
07/02/2019	1.8E	● GW1N-6/9 MG196, UG169, and EQ144 added. ● GW1N-1S CS30 added.
10/10/2019	1.9E	● GW1N-1 LQ100X-LV and LQ100X-UV added. ● BSRAMs in GW1N-1S do not support Dual port mode. ● The package sizes of LQ100 / LQ144 / EQ144 / LQ176 / EQ176 fixed. ● Junction temperature of automotive operation added. ● Power supply ramp rates updated.
11/15/2019	2.0E	● The number of Maximum I/Os updated. ● Automotive grade description added to 5.1 Part Name. ● IODELAY description added.
01/15/2020	2.1E	● The package name of LQ100X-LV and LQ100X-UV updated. ● GW1N-4 MG132X added.
03/16/2020	2.2E	● GW1N-9 CS81M added. ● Description of PLL CLKIN frequency updated.
04/16/2020	2.3E	● GW1N-2/GW1N-2B/GW1N-6 removed. ● CFU view updated. ● GW1N-9C added.
09/30/2020	2.4E	● GW1N-2 added. ● GW1N-9 MG100 added. ● GW1N-9 QN48F added.
04/06/2021	2.5E	GW1N-1P5 added.
05/27/2021	2.6E	● GW1N-1P5 LQ100 added. ● GW1N-2 MG132/LQ100/LQ144 added. MG132 renamed to MG132H, QN48M renamed to QN48H. ● GW1N-9 MG100T added. ● GW1N-1 LQ100X removed.

Date	Version	Description
		● “Table 2-3 Configuration Modes Supported by Different Packages” added.
05/20/2022	2.7E	● GW1N-4 UG169 added. ● GW1N-2 CS42H updated. ● The drive strength of MIPI IOs updated. ● Recommended I/O operating conditions updated. ● On-chip oscillator frequency updated. ● Gearbox internal timing parameters updated.
06/02/2022	2.7.1E	GW1N-1 QN32/QN48/LQ100/LQ144 added.
06/23/2022	2.7.2E	GW1N-1 CS30/FN32 removed.
07/01/2022	2.7.3E	GW1N-1 CS30 added.
07/21/2022	2.8E	● GW1N-2 QN32 added. ● GW1N-2 CS100H added. ● GW1N-2 LQ144F added. ● The maximum value of the differential input threshold V_{THD} updated. ● Note about loading frequency for the GW1N-2 device added. ● Description of configuration modes supported by GW1N-1 CS30 added. ● GW1N-1S CS30/FN32 removed.
08/18/2022	2.8.1E	GW1N-1 QN32/QN48/LQ100/LQ144 removed.
09/29/2022	2.9E	● Note about DC current limit added. ● Table 3-2 Recommended Operating Conditions updated. ● Note about Vcc of GW1N-4/GW1N-9 UV version devices added. ● Architecture overviews updated. ● Table 3-5 POR Parameters updated. ● Table 3-9 Static Current updated. ● 3.4 Switching Characteristics updated.
11/11/2022	2.9.1E	● Table 3-3 Power Supply Ramp Rates updated. ● Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions updated. ● Description of configuration Flash added. ● Note about byte-enable added.
11/21/2022	2.9.2E	● Table 3-1 Absolute Max. Ratings updated. ● Table 3-9 Static Current updated. ● Description of the background upgrade feature in section 2.12Programming & Configuration updated.
12/08/2022	2.9.3E	● Table 3-1 Absolute Max. Ratings updated. ● Table 3-22 GW1N-1 User Flash DC Characteristics updated. ● Table 3-23 GW1N-2/4/9 User Flash DC Characteristics(I) added. ● Table 3-24 GW1N-2/4/9 User Flash DC Characteristics(II)[1], [4] updated. ● Note for Table 2-5 BSRAM Size Configuration modified.
12/19/2022	2.9.4E	GW1N-1P5 QN48XF added.
01/12/2023	2.9.5E	● Table 1-2 Device-Package Combinations and Maximum User I/Os (True LVDS Pairs updated.

Date	Version	Description
		● Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions updated.
02/22/2023	2.9.6E	● Information on Slew Rate removed. ● Table 3-26 GW1N-1P5/2/4/9 User Flash Parameters updated. ● Description added to 2.5User Flash(GW1N-1) and 2.6User Flash(GW1N-1P5/2/4/9). ● Description of true LVDS design modified.
04/13/2023	2.9.7E	● Note about the default state of GPIOs modified. ● Note for Figure 2-5 CFU Structure View modified. ● Table 3-3 Power Supply Ramp Rates updated. ● The I/O logic output diagram and the I/O logic input diagram combined into Figure 2-12 I/O Logic Input and Output. ● Description of MIPI input/output updated.
04/27/2023	2.9.8E	● Description of Flash resources updated. ● Note for Table 2-5 BSRAM Size Configuration modified. ● Description of the V_{CCIO} power supply restrictions of the GW1N-9 device updated.
05/25/2023	2.9.9E	Section 2.4.2 BSRAM Configuration Modes added.
06/09/2023	3.0E	Table 2-9 List of GW1N series of FPGA Products that Support MIPI IO added.
08/18/2023	3.1E	● Note for Table 1-2 Device-Package Combinations and Maximum User I/Os (True LVDS Pairs optimized. ● Note for Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions modified. ● Table 3-26 GW1N-1P5/2/4/9 User Flash Parameters updated. ● Figure 4-3 Package Marking Examples updated. ● Note about the default state of GPIOs optimized. ● Editorial updates.
11/30/2023	3.2E	● GW1N-1 QN32/QN48/LQ100/LQ144 removed. ● Table 1-1 Product Resources updated. ● Section 2.4.7 Power up Conditions removed. ● Note added toTable 2-1 Output I/O Standards and Configuration Options and Table 3-12 Single-ended I/O DC Characteristics. ● Note added to Table 3-2 Recommended Operating Conditions. ● Table 3-17 Gearbox Timing Parameters optimized. ● Description of the V_{CCIO} power supply restrictions of the GW1N-9 device optimized. ● Description of Flash resources updated.
12/14/2023	3.2.1E	Table 1-2 Device-Package Combinations and Maximum User I/Os (True LVDS Pairs) updated, correcting the numbers of maximum user IOs of the GW1N-2 device in CS42H and CS100H packages.
02/02/2024	3.2.2E	● “Table 1-2 Device-Package Combinations and Maximum User I/Os (True LVDS Pairs)” updated, correcting size information of GW1N-1 CS30. ● Note added to “Table 2-5 BSRAM Size Configuration” , adding information on devices that do not support ROM mode. ● “Table 3-1 Absolute Max. Ratings” and “Table 3-2 Recommended Operating Conditions” updated, adding voltage

Date	Version	Description
		information for hard core MIPI D-PHY.
03/12/2024	3.2.3E	● Description of Bank6 in “Figure 2-9 I/O Bank Distribution View of GW1N-2” added. ● Static currents of GW1N-4 in “Table 3-9 Static Current” updated. ● “Table 3-17 Gearbox Timing Parameters” updated.
05/09/2024	3.2.4E	● Note on Maximum GPIOs added to “Table 1-1 Product Resources”. ● Description of IODELAY module updated. ● “Table 3-12 Single-ended I/O DC Characteristics” updated, modifying I_{OL} and I_{OH} of LVCMOS12 standard. ● “Figure 4-4 Package Marking Examples(GW1N-LV4CS72C6/I5)”
12/12/2024	3.2.5E	● Note on functional description of dual port BSRAM and semi-dual port BSRAM modified. ● “Table 3-12 Single-ended I/O DC Characteristics” updated, modifying I_{OL} and I_{OH} of LVCMOS12 standard. ● Description of MIPI IO clarified.
04/30/2025	3.2.6E	● “Table 2-1 Output I/O Standards and Configuration Options” updated: correcting drive strength values for some I/O types. ● “Table 2-2 Input I/O Standards and Configuration Options” updated: modifying V_{CCIO} values for some I/O types. ● “Table 3-16 DSP Timing Parameters”updated：removing information on GW1N-1, GW1N-1S, GW1N-1P5, and GW1N-2. ● “3.4.7 PLL Switching Characteristics” updated. ● GW1N-9 CS81M removed.
05/23/2025	3.2.7E	● “Table 3-21 PLL Timing Parameters” updated. ● Notes for “Figure 4-3 Package Marking Examples” and “Figure 4-4 Package Marking Examples(GW1N-LV4CS72C6/I5)” updated.
06/27/2025	3.2.8E	“Table 2-2 Input I/O Standards and Configuration Options” optimized.
08/29/2025	3.3E	● “Table 3-18 Single-ended IO Fmax” optimized. ● Note added to“Table 2-5 BSRAM Size Configuration”。 ● Note for “Table 3-26 GW1N-1P5/2/4/9 User Flash Parameters[1], [4], [5]”updated. ● GW1N-9 QN60 updated.
12/31/2025	3.3.1E	● EOL note for GW1N-2 LQ144F added. ● “Figure 2-19 GW1N-1 HCLK Distribution”, “Figure 2-20 GW1N-1P5/2 HCLK Distribution”, “Figure 2-21 GW1N-4 HCLK Distribution”, “Figure 2-22 GW1N-9 HCLK Distribution” optimized. ● “Table 3-21 PLL Timing Parameters” updated: adding information on GW1N-1P5.
03/27/2026	3.3.2E	● “Table 1-1 Product Resources” updated：adding information on hard MIPI D-PHY RX support. ● “Table 5-1 Terminology and Abbreviations” updated：adding entry CLU.
06/17/2026	3.3.3E	● Information on GW1N-1S removed. ● Description of IEM module removed. ● “Table 1-2 Device-Package Combinations and Maximum User

Date	Version	Description
		I/Os (True LVDS Pairs)" updated：standardizing the counting criteria for the maximum user I/O count. ● "Table 3-14 CFU Internal Timing Parameters[1], [2]" updated. ● "Figure 2-19 GW1N-1 HCLK Distribution", "Figure 2-20 GW1N-1P5/2 HCLK Distribution", "Figure 2-21 GW1N-4 HCLK Distribution", "Figure 2-22 GW1N-9 HCLK Distribution" optimized. ● Electrical parameters for C7/I6 GW1N-4 removed.
11/13/2026	3.3.4E	● Updated "Figure 2-5 CFU Structure View". ● Removed description of barrel shifter function of DSP block. ● Updated name and link for physical constraints manual.

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1 General Description

The GW1N series of FPGA products are the first generation products in the LittleBee family. They offer abundant logic resources, multiple I/O standards, embedded BSRAMs, DSPs, PLLs, and built-in Flashes. They are non-volatile FPGA products featuring low power, instant-on, low cost, enhanced security, small footprint, various packaging options, and flexible usage.

GOWINSEMI provides a new generation of FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

1.1 Features

- Lower power consumption
  - 55nm embedded flash technology
  - LV: Supports 1.2V core voltage
  - UV: Supports unique power supplies for V_{CC}/ V_{CCIO}/ V_{CCX}
  - Supports dynamically turning on/off the clock
- User Flash (GW1N-1)
  - NOR Flash
  - 100,000 write cycles
  - Greater than 10 years of data retention at +85℃
  - Selectable input/output data widths of 8/16/32 bits
  - Page size: 256 bytes
  - Standby current: 3μA
  - Page write time: 8.2ms
- User Flash（GW1N-1P5/2/4/9）
  - NOR Flash
  - 10,000 write cycles
  - Greater than 10 years of data retention at +85℃
  - Data width: 32 bits
  - Capacity in GW1N-1P5/2: 96 Kbits
  - Capacity in GW1N-4: 256 Kbits
  - Capacity in GW1N-9: 608 Kbits
  - Page Erase Capability: 2,048 bytes per page
  - Word Program Time: ≤16μs
  - Page Erase Time: ≤120ms
- Configuration Flash (GW1N-1)
  - NOR Flash
  - 100,000 write cycles

  - Greater than 10 years of data retention at +85℃
- Configuration Flash（GW1N-1P5/2/4/9）
  - NOR Flash
  - 10,000 write cycles
  - Greater than 10 years of data retention at +85℃
- Hard MIPI D-PHY RX core(GW1N-2)
  - Supports MIPI DSI and MIPI CSI-2 RX
  - IO Bank6 in CS42, CS42H, QN48H, QN88, MG132H, and CS100H packages supports MIPI D-PHY RX
  - MIPI data rate up to 2Gbps per lane
  - Supports up to 4 data lanes and 1 clock lane
- MIPI D-PHY RX/TX Implemented by Using GPIOs
  - Supports MIPI CSI-2 and MIPI DSI RX/TX with a data rate of up to 1.2Gbps per lane
  - Three IO types are available：TLVDS, ELVDS, and MIPI IO
- Multiple I/O standards
  - LVCMOS33/25/18/15/12；LVTTL33, SSTL33/25/18 I, SSTL33/25/18 II，SSTL15；HSTL18 I, HSTL18 II, HSTL15 I；PCI, LVDS25, RSDS, LVDS25E, BLVDSE, MLVDSE, LVPECLE, RSDSE
  - Input hysteresis options
  - Drive strength options
  - Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
  - Hot socketing
- High-performance DSP blocks(GW1N-4/9)
  - High-performance digital signal processing
  - Supports 9 x 9,18 x 18,36 x 36 bit multipliers and 54-bit accumulators
  - Supports cascading of multipliers
  - Supports pipeline mode and bypass mode
  - Pre-addition operation for the filter function
- Abundant basic logic cells
  - 4-input LUTs (LUT4s)
  - Supports shift registers and shadow SRAMs
- Block SRAMs with multiple modes
  - Supports Dual Port mode, Single Port mode, and Semi-Dual Port mode
  - Supports byte-enable
- Flexible PLLs
  - Frequency adjustment (multiplication and division) and phase adjustment
  - Supports global clocks
- Built-in Flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration
  - Supports background upgrade

- Supports up to seven GowinCONFIG configuration modes:	AUTOBOOT, SSPI, MSPI, CPU, SERIAL, DUAL BOOT, I2C Slave

1.2 Product Resources

Table 1-1 Product Resources

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
LUT4s	1,152	1,584	2,304	4,608	8,640
Flip-Flops (FFs)	864	1,584	2,016	3,456	6,480
Shadow SRAM(SSRAM) Capacity (bits)	0	12K	18K	0	16K
Block SRAM(BSRAM) Capacity(bits)	72K	72K	72K	180K	468K
Number of BSRAMs	4	4	4	10	26
User Flash(bits)	96K	96K	96K	256K	608K
Multipliers(18 x 18 Multipliers)	0	0	0	16	20
Hard MIPI D-PHY RX Core[5]	0	0	1	0	0
PLLs	1	1	1	2	2
I/O Banks	4	6	6[2]	4	4
Maximum GPIOs[4]	120	125	125	218	276
Core Voltage (LV Version)	1.2V	1.2V	1.2V	1.2V	1.2V
Core Voltage (UV Version)	1.8V/2.5V/3.3V[1]	1.8V/2.5V/3.3V		1.8V[3]/2.5V/3.3V	

Note!

- [1] For the GW1N-1 device, only the LQ100X package supports the UV version at present.
- [2] The GW1N-2 device in the CS42/QN48H/MG132H/QN88/CS42H/CS100H packages has seven IO banks.
- [3] For UV version GW1N-4/GW1N-9 devices, if V_{CC} and Vccx share a pin in a package, the Vccx range (2.5V~3.3V) of GW1N-4/GW1N-9 will limit the Vcc range to 2.5 V~3.3V, in this case Vcc does not support 1.8V.

- [4] This is the maximum number of GPIOs the device can provide without package limitation. Please refer to Table 1-2 for the maximum number of user I/Os available for the specific packages.
- [5] Currently, the GW1N-2 device in the CS42/QN48H/MG132H/QN88/CS42H/CS100H packages supports hard MIPI D-PHY RX.

1.3 Package Information

Table 1-2 Device-Package Combinations and Maximum User I/Os (True LVDS Pairs)

Package	Pitch(mm)	Size(mm)	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
CM64	0.5	4.1 x 4.1	-	-		-	56（16）
CS100H	0.4	4 x 4	-	-	79（21）	-	-
CS30[1]	0.4	2.3 x 2.2	24	-	-	-	-
CS42	0.4	2.4 x 2.9	-	-	25（7）	-	-
CS42H	0.4	2.4 x 2.9	-	-	21（3）	-	-
CS72	0.4	3.6 x 3.3	-	-	-	58（19）	-
EQ144	0.5	20 x 20	-	-	-	-	121（28）
EQ176	0.4	20 x 20	-	-	-	-	148（37）
FN32	0.4	4 x 4	-	-		-	-
LQ100	0.5	14 x 14	-	81（16）	81（15）	80（13）	80（20）
LQ100X	0.5	14 x 14	-	81（16）	81（15）	-	-
LQ144	0.5	20 x 20	-	-	114（28）	120（22）	121（28）
LQ144F[2]	0.5	20 x 20	-	-	116（27）	-	-
LQ144X	0.5	20 x 20	-	-	114（28）	-	-
LQ176	0.4	20 x 20	-	-	-	-	148（37）
MG100	0.5	5 x 5	-	-	-	-	88（25）
MG100T	0.5	5 x 5	-	-	-	-	88（17）
MG121	0.5	6 x 6	-	-	101（28）	-	-
MG121X	0.5	6 x 6	-	-	101（28）	-	-
MG132	0.5	8 x 8	-	-	105（29）	-	-

Package	Pitch(mm)	Size(mm)	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
MG132H	0.5	8 x 8	-	-	95（29）	-	-
MG132X	0.5	8 x 8	-	-	105 (29)	106（23）	-
MG160	0.5	8 x 8	-	-	-	132（25）	132（38）
MG196	0.5	8 x 8	-	-	-	-	114（35）
MG49	0.5	3.8 x 3.8	-	-	42（11）	-	-
PG256	1.0	17 x 17	-	-	-	208（32）	208（36）
PG256M	1.0	17 x 17	-	-	-	208（32）	-
QN32	0.5	5 x 5	-	-	22（1）	24（3）	-
QN32X	0.5	5 x 5	-	-	22（1）	-	-
QN48	0.4	6 x 6	-	-	41（12）	41（9）	41（12）
QN48F	0.4	6 x 6	-	-	-	-	40（11）
QN48H	0.4	6 x 6	-	-	31（8）	-	-
QN48X	0.5	7 x 7	-	40（10）	-	-	-
QN48XF	0.5	7 x 7	-	40（11）	-	-	-
QN60	0.35	6 x 6	-	-	-	-	45（11）
QN88	0.4	10 x 10	-	-	58（17）	71（11）	71（19）
UG169	0.8	11 x 11	-	-	-	130（27）	130（38）
UG256	0.8	14 x 14	-	-	-	-	208（36）
UG332	0.8	17 x 17	-	-	-	-	274（43）

Note!

- When JTAGSEL_N and the JTAG pins (TCK, TMS, TDI, TDO) are multiplexed as GPIOs simultaneously, note that a low-level JTAGSEL_N (input or output) will force the JTAG pins to revert to dedicated configuration I/Os. However, this behavior does not apply when mode[2:0] = 001 (input or output).
- The package types in this manual are referred to by acronyms, see 4.1 Part Naming for more information.
- [1] GW1N-1 CS30 only supports SSPI mode.
- [2] GW1N-2 LQ144F is an EOL package.

Table1-3 Configuration Modes Supported by Different Packages(GW1N-1P5, GW1N2)

Device	Package	Mode[2:0]	Configuration Mode	Notes
GW1N-2[1]	QN32 CS42 LQ100 LQ144 LQ144F MG121 MG132	000	JTAG Autoboot	–
	LQ100X LQ144X MG121X MG132X MG49 QN32X CS42H	100	JTAG I²C Autoboot	When I²C is supported, the SDA and SCL pins need to be pulled up externally. When Mode[2:0] is configured as 100 and Autoboot is used, the SDA pin needs to be pulled up externally.
	QN48 QN48H	00X	JTAG Autoboot SSPI	–
	MG132H CS100H	X0X	JTAG I²C Autoboot SSPI	When I²C is supported, the SDA and SCL pins need to be pulled up externally. When Mode[2,0] is configured as 100 and Autoboot is used, the SDA pin needs to be pulled up externally.
	QN88	XXX	JTAG I²C Autoboot SSPI MSPI DUAL BOOT SERIAL CPU	–

Device	Package	Mode[2:0]	Configuration Mode	Notes
GW1N-1P5	LQ100X QN48X	100	JTAG I²C Autoboot	When I²C is supported, the SDA and SCL pins need to be pulled up externally. When Mode[2,0] is configured as 100 and Autoboot is used, the SDA pin needs to be pulled up externally.
	LQ100 QN48XF	000	JTAG Autoboot	–

Note!

[1] For the GW1N-2 device, if its MODE[2] value is fixed to 1, its loading frequency can only be 2.5MHz.

2 Architecture

2.1 Architecture Overview

Figure 2-1 Architecture Overview of GW1N-9

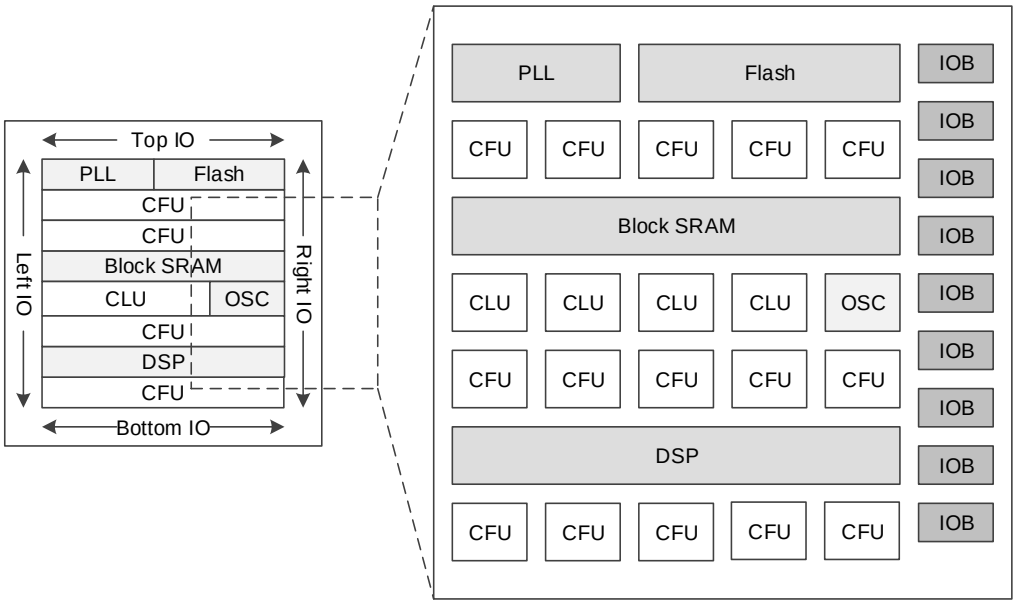


Figure 2-2 Architecture Overview of GW1N-4

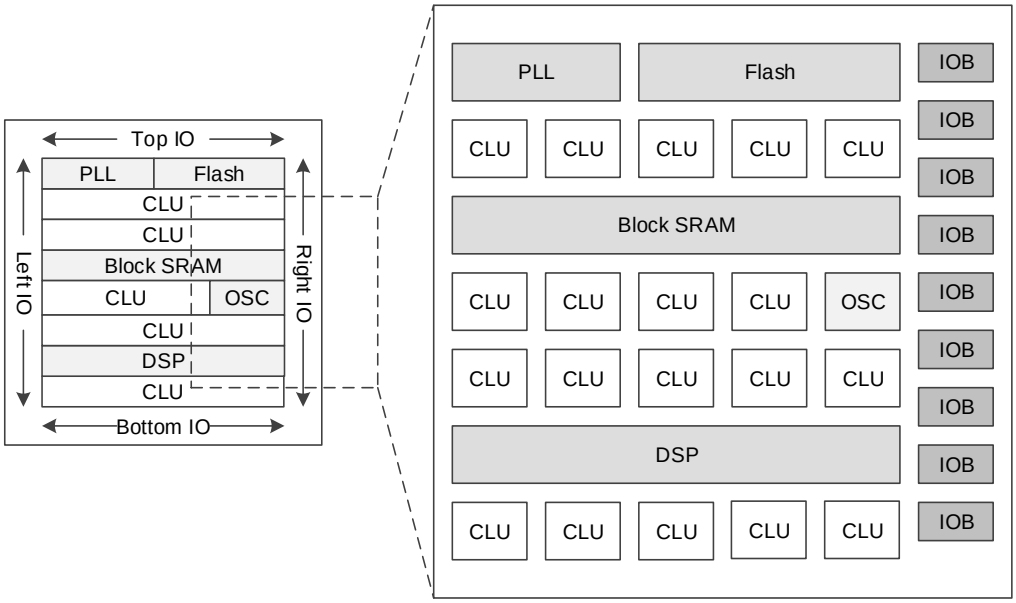


Figure 2-3 Architecture Overview of GW1N-1

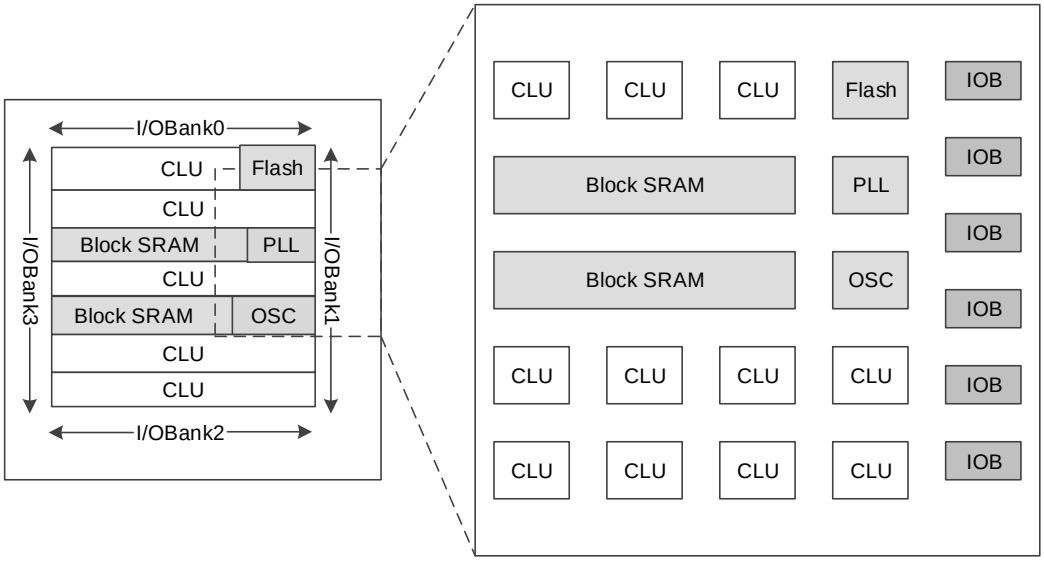
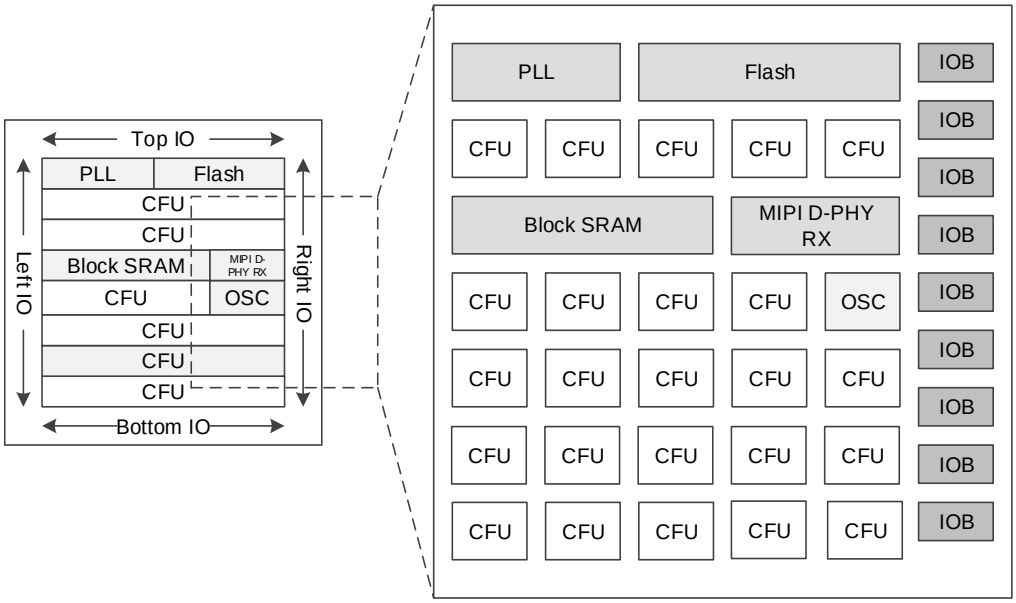


Figure2-4 Architecture Overview of GW1N-2



As shown in Figure 2-1 to Figure 2-3, the core of the FPGA is an array of logic cells surrounded by IO blocks. Besides, BSRAMs, DSP blocks, PLLs, an on-chip oscillator, and Flash resources that support instant-on are provided. As shown in Figure2-4, the GW1N-2 device is further embedded with a hard MIPI D-PHY RX core compared with other GW1N devices. See Table 1-1 for more information on the resources provided.

The Configurable Function Unit (CFU) and the Configurable Logic Unit (CLU) are the two kinds of basic logic blocks that form the core of Gowin FPGAs. Devices with different capacities have different numbers of rows and columns of CFUs/CLUs. See 2.2 Configurable Function Units for more information.

The I/O resources in the GW1N series of FPGA products are arranged around the periphery of the devices in groups referred to as banks. The I/O resources support multiple I/O standards and can be used for regular mode, SDR mode, and generic DDR mode. For more information, see 2.3 Input/Output Blocks.

BSRAMs are embedded as a row in the GW1N series of FPGA products. Each BSRAM has a capacity of 18 Kbits and supports multiple configuration modes and operation modes. For more information, see 2.4 Block SRAM.

GW1N-1/1P5/2, GW1N-4, and GW1N-9 feature embedded Flash resources with capacities of 1 Mbits, 2 Mbits, and 4 Mbits respectively. The Flash memory resources consist of configuration Flash resources and user Flash resources. Configuration Flash resources are used for internal Flash programming, see 2.12 Programming & Configuration for more information. User Flash resources are used for user storage, see 2.5 User Flash(GW1N-1) and 2.6 User Flash(GW1N-1P5/2/4/9) for more information.

GW1N-4 and GW1N-9 provide DSP blocks. Each DSP block contains two macros, and each macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU. For more information, see 2.7 Digital Signal Processing.

Note!

GW1N-1 and GW1N-2 do not support DSP resources currently.

The GW1N series of FPGA products have embedded PLL resources. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be realized by the configuration of parameters. In addition, an programmable on-chip oscillator is provided, see 2.9 Clock and 2.13 On-chip Oscillator for more information.

The GW1N-2 device contains a hard MIPI D-PHY RX core, see 2.8 MIPI D-PHY for more information.

There are also abundant Configurable Routing Units (CRUs) that interconnect all the resources within the FPGA. For example, routing resources distributed in CFUs and IOBs interconnect resources in them. Routing resources can be automatically generated by the Gowin software. In addition, the GW1N series of FPGA products also provide abundant dedicated clock resources, long wires (LWs), global set/reset (GSR) resources, programming options, etc. For more information, see 2.9 Clock, 2.10 Long Wires, and 2.11 Global Set/Reset.

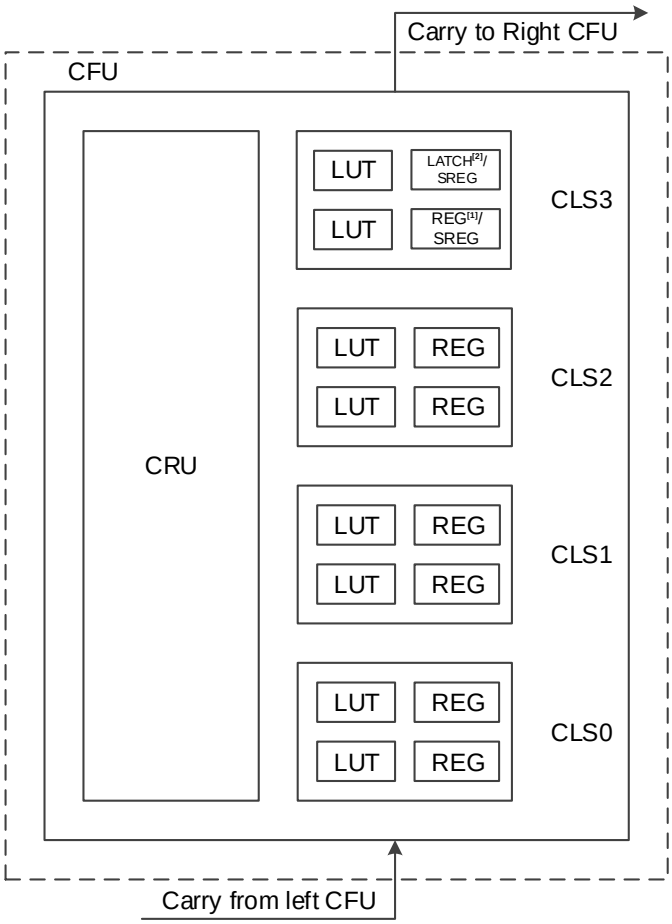
2.2 Configurable Function Units

Configurable Function Units (CFUs) and/or Configurable Logic Units (CLUs) are the basic cells that make up the core of Gowin FPGAs. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs), with three of the CLSs each containing two 4-input LUTs and two registers, and the remaining one only containing two 4-input LUTs, as shown in Figure 2-5 .

The CLSs in the CLUs cannot be configured as SRAMs, but can be configured as basic LUTs, ALUs, and ROMs. The CLSs in the CFUs can be configured as basic LUTs, ALUs, SRAMs, and ROMs according to application scenarios.

For more information on the CFUs, see UG288, Gowin Configurable Function Unit (CFU) User Guide.

Figure 2-5 CFU Structure View



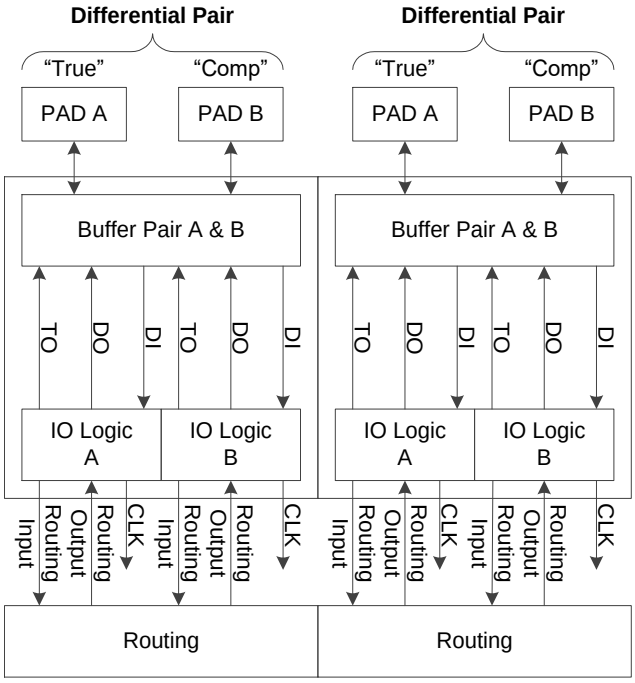
Note!

- The SREGs need special patch support. Please contact Gowin's technical support or local office for this patch.
- Currently, only GW1N-1P5 and GW1N-2 support the REG in CLS3, and the CLK, CE, and SR of CLS3 and CLS2 are driven by the same source.
- Currently, only GW1N-1P5 and GW1N-2 support the LATCH in CLS3.

2.3 Input/Output Blocks

The Input/Output Block (IOB) in the GW1N series of FPGA products consists of a buffer pair, IO logic, and corresponding routing units. As shown below, each IOB connects to two pins (marked as A and B), which can be used as a differential pair or as two single-ended inputs/outputs.

Figure 2-6 IOB Structure View



The features of the IOB include:

- V_{CCIO} supplied with each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, HSTL, etc.
- Input hysteresis options
- Drive strength options
- Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
- Hot socketing
- IO logic supports basic mode, SDR mode, DDR mode, etc.

Note!

- The GW1N series of FPGA products support MIPI IO type, see Table 2-9 for more details.
- GW1N-1 does not support true LVDS output.
- 2.3.1~ 2.3.4 describe I/O standards, true LVDS design, I/O logic, and I/O logic modes. For more information about the IOB, please refer to UG289,Gowin Programmable IO (GPIO) User Guide.

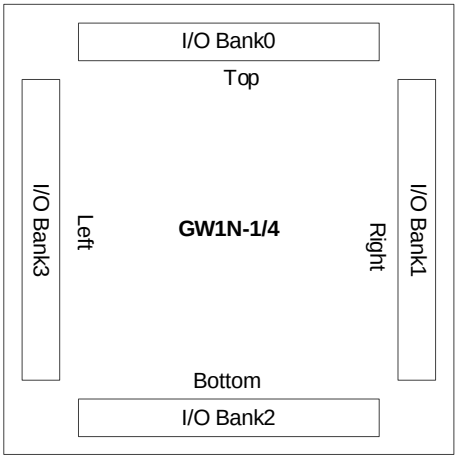
2.3.1 I/O Standards

Each Bank has its own I/O power supply V_{CCIO}.

To support SSTL, HSTL, etc., each bank also has one independent voltage source (V_{REF}) as the reference voltage. You can choose to use the internal V_{REF} (0.5 x V_{CCIO}) or the external V_{REF} input via any IO from the bank.

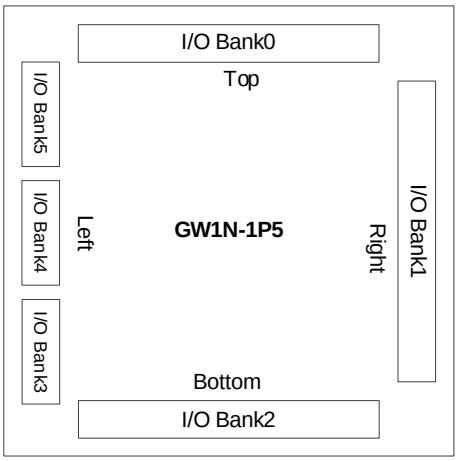
There are four IO banks in the GW1N-1/4 devices, as shown in Figure 2-7.

Figure 2-7 I/O Bank Distribution View of GW1N-1/4



There are six IO banks in the GW1N-1P5 device, as shown in Figure 2-8.

Figure 2-8 I/O Bank Distribution View of GW1N-1P5

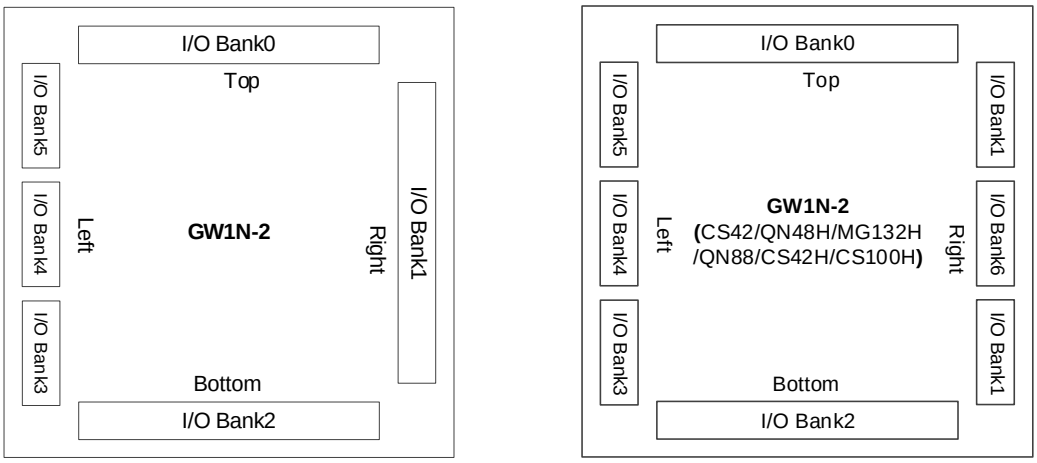


There are six banks in the GW1N-2 device, while in the case of GW1N-2 in the CS42, QN48H, MG132H, QN88, CS42H and CS100H packages, there are seven banks, of which Bank6[1] is a dedicated MIPI Bank for MIPI D-PHY RX, as shown in Figure 2-9.

Note!

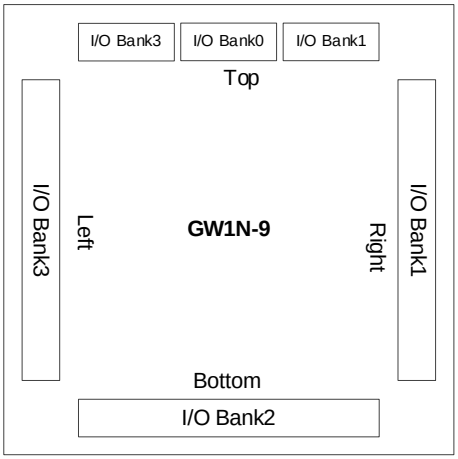
[1] If the MIPI function is not used, the pins of Bank6 can be left floating. Bank6 can also be used for differential inputs (with common mode voltage ≤ 0.5V) by bypassing the MIPI logic.

Figure 2-9 I/O Bank Distribution View of GW1N-2



There are four IO banks in the GW1N-9 device, as shown in Figure 2-10.

Figure 2-10 I/O Bank Distribution View of GW1N-9



The GW1N series of FPGA products are available in LV version and UV version.

The LV version devices support 1.2V V_{CC} for low power consumption. V_{CCIO} can be set to 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V as needed.

The UV version devices support 1.8V, 2.5V, and 3.3V V_{CC}, and a linear voltage regulator is integrated to facilitate a single power supply.

V_{CCX} can be 2.5V or 3.3V.

The GPIOs of the GW1N series of FPGA products support MIPI IO type, see Table 2-9 for more information.

Note!

- During configuration, all GPIOs of the device are high-impedance with internal weak pull-ups. After the configuration is complete, the I/O states are controlled by user programs and constraints. The states of configuration-related I/Os differ depending on the configuration mode.

- For the recommended operating conditions of different devices, please refer to 3.1 Operating Conditions.
- When the I/Os of Bank0/Bank3/Bank4/Bank5 of GW1N-2/GW1N-1P5 are used as MIPI output, V_{CCIO0}/V_{CCIO3}/V_{CCIO4}/V_{CCIO5} need to be supplied with a 1.2V power supply.
- When the I/Os of Bank2 of GW1N-2/GW1N-1P5 are used as MIPI input, V_{CCIO2} needs to be supplied with a 1.2V power supply.
- When the I/Os of Bank0 of GW1N-9 are used as MIPI input, V_{CCIO0} needs to be supplied with a 1.2V power supply.
- When the I/Os in Bank2 of GW1N-9 are used as MIPI output, V_{CCIO2} needs to be supplied with a 1.2V power supply.
- The I/O power supply restrictions for Bank0/Bank1/Bank3 in GW1N-9(For the C version of the GW1N-9 device, there are no such power supply restrictions):
  - When V_{CCIO0} is greater than or equal to 1.8V, V_{CCIO1} and V_{CCIO3} support 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
  - When V_{CCIO0} is 1.5V, V_{CCIO1} and V_{CCIO3} support 1.2V, 1.5V, 1.8V, and 2.5V.
  - When V_{CCIO0} is 1.2V, V_{CCIO1} and V_{CCIO3} support 1.2V, 1.5V, and 1.8V.

For the V_{CCIO} requirements of different I/O standards, see Table 2-1 and Table 2-2.

Table 2-1 Output I/O Standards and Configuration Options

I/O Standard (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
MIPI[1]	Differential (TLVDS)	1.2	3.5	Mobile Industry Processor Interface
LVDS25[2]	Differential (TLVDS)	2.5/3.3	2.5/3.5/4.5/6(GW1N-1P5/2), 1.25/2/2.5/3.5(GW1N-4/9)	High-speed point-to-point data transmission
RSDS[2]	Differential (TLVDS)	2.5/3.3	2.5(GW1N-1P5/2), 1.25/2/2.5/3.5(GW1N-4), 2(GW1N-9)	High-speed point-to-point data transmission
MINILVDS[2]	Differential (TLVDS)	2.5/3.3	2.5(GW1N-1P5/2), 1.25/2/2.5/3.5(GW1N-4), 2(GW1N-9)	LCD timing driver interface and column driver interface
PPLVDS[2]	Differential (TLVDS)	2.5/3.3	3.5(GW1N-1P5/2/9), 1.25/2/2.5/3.5(GW1N-4)	LCD row/column driver
LVDS25E	Differential	2.5	8	High-speed point-to-point data transmission
BLVDS25E	Differential	2.5	16	Multi-point high-speed data transmission
MLVDS25E	Differential	2.5	16	LCD timing driver interface and column driver interface
RSDS25E	Differential	2.5	8	High-speed point-to-point data transmission
LVPECL33E	Differential	3.3	16	Universal interface
HSTL18D_I	Differential	1.8	8	Memory interface
HSTL18D_II	Differential	1.8	8	Memory interface
HSTL15D_I	Differential	1.5	8	Memory interface
SSTL15D	Differential	1.5	8	Memory interface

I/O Standard (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
SSTL18D_I	Differential	1.8	8	Memory interface
SSTL18D_II	Differential	1.8	8	Memory interface
SSTL25D_I	Differential	2.5	8	Memory interface
SSTL25D_II	Differential	2.5	8	Memory interface
SSTL33D_I	Differential	3.3	8	Memory interface
SSTL33D_II	Differential	3.3	8	Memory interface
LVCMOS12D	Differential	1.2	4/8	Universal interface
LVCMOS15D	Differential	1.5	4/8	Universal interface
LVCMOS18D	Differential	1.8	4/8/12	Universal interface
LVCMOS25D	Differential	2.5	4/8/12/16	Universal interface
LVCMOS33D	Differential	3.3	4/8/12/16(GW1N-1P5/2), 4/8/12/16/24(GW1N-1/4/9)	Universal interface
HSTL15_I	Single-ended	1.5	8	Memory interface
HSTL18_I	Single-ended	1.8	8	Memory interface
HSTL18_II	Single-ended	1.8	8	Memory interface
SSTL15	Single-ended	1.5	8	Memory interface
SSTL18_I	Single-ended	1.8	8	Memory interface
SSTL18_II	Single-ended	1.8	8	Memory interface
SSTL25_I	Single-ended	2.5	8	Memory interface
SSTL25_II	Single-ended	2.5	8	Memory interface
SSTL33_I	Single-ended	3.3	8	Memory interface
SSTL33_II	Single-ended	3.3	8	Memory interface
LVCMOS12	Single-ended	1.2	2/6(GW1N-1P5/2), 4/8(GW1N-1/4/9)	Universal interface
LVCMOS15	Single-ended	1.5	4/8	Universal interface
LVCMOS18	Single-ended	1.8	4/8/12	Universal interface
LVCMOS25	Single-ended	2.5	4/8/12/16	Universal interface

I/O Standard (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
LVCMOS33/ LVTTL33	Single-ended	3.3	4/8/12/16(GW1N-1P5/2), 4/8/12/16/24(GW1N-1/4/9)	Universal interface
PCI33	Single-ended	3.3	4/8	PC and embedded system

Note!

- [1] Bank0/Bank3/Bank4/Bank5 of GW1N-2/GW1N-1P5 and Bank2 of GW1N-9 support MIPI I/O output.
- [2] GW1N-1 does not support this I/O type.

Table 2-2 Input I/O Standards and Configuration Options

I/O Standard (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis Options Supported?	V_{REF} Required?
MIPI[1]	Differential （TLVDS）	1.2	No	No
LVDS25	Differential （TLVDS）	2.5/3.3	No	No
RSDS	Differential （TLVDS）	2.5/3.3	No	No
MINILVDS	Differential （TLVDS）	2.5/3.3	No	No
PPLVDS	Differential （TLVDS）	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33E	Differential	3.3	No	No
HSTL18D_I	Differential	1.8	No	No
HSTL18D_II	Differential	1.8	No	No
HSTL15D_I	Differential	1.5	No	No
SSTL15D	Differential	1.5	No	No
SSTL18D_I	Differential	1.8	No	No

I/O Standard (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis Options Supported?	V_{REF} Required?
SSTL18D_II	Differential	1.8	No	No
SSTL25D_I	Differential	2.5	No	No
SSTL25D_II	Differential	2.5	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
LVCMOS12D	Differential	1.2	No	No
LVCMOS15D	Differential	1.5	No	No
LVCMOS18D	Differential	1.8	No	No
LVCMOS25D	Differential	2.5	No	No
LVCMOS33D	Differential	3.3	No	No
HSTL15_I	Single-ended	1.5	No	Yes
HSTL18_I	Single-ended	1.8	No	Yes
HSTL18_II	Single-ended	1.8	No	Yes
SSTL15	Single-ended	1.5	No	Yes
SSTL18_I	Single-ended	1.8	No	Yes
SSTL18_II	Single-ended	1.8	No	Yes
SSTL25_I	Single-ended	2.5	No	Yes
SSTL25_II	Single-ended	2.5	No	Yes
SSTL33_I	Single-ended	3.3	No	Yes
SSTL33_II	Single-ended	3.3	No	Yes
LVCMOS12[2]	Single-ended	1.2	Yes	No
LVCMOS12UD15[2],[3]	Single-ended	1.5	No	No
LVCMOS12UD18[2],[3]	Single-ended	1.8	No	No
LVCMOS12UD25[2],[3]	Single-ended	2.5	No	No
LVCMOS12UD33[2],[3]	Single-ended	3.3	No	No
LVCMOS15OD12[2],[3]	Single-ended	1.2	No	No
LVCMOS15[2]	Single-ended	1.5	Yes	No

I/O Standard (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis Options Supported?	V_{REF} Required?
LVCMOS15UD18[2],[3]	Single-ended	1.8	No	No
LVCMOS15UD25[2],[3]	Single-ended	2.5	No	No
LVCMOS15UD33[2],[3]	Single-ended	3.3	No	No
LVCMOS18OD15[2],[3]	Single-ended	1.5	No	No
LVCMOS18[2]	Single-ended	1.8	Yes	No
LVCMOS18UD25[2],[3]	Single-ended	2.5	No	No
LVCMOS18UD33[2],[3]	Single-ended	3.3	No	No
LVCMOS25OD15[2],[3]	Single-ended	1.5	No	No
LVCMOS25OD18[2],[3]	Single-ended	1.8	No	No
LVCMOS25[2]	Single-ended	2.5	Yes	No
LVCMOS25UD33[2],[3]	Single-ended	3.3	No	No
LVCMOS33OD15[2],[3]	Single-ended	1.5	No	No
LVCMOS33OD18[2],[3]	Single-ended	1.8	No	No
LVCMOS33OD25[2],[3]	Single-ended	2.5	No	No
LVCMOS33[2]	Single-ended	3.3	Yes	No
LVTTL33	Single-ended	3.3	Yes	No
PCI33	Single-ended	3.3	Yes	No

Note!

- [1] Bank2 of GW1N-2/GW1N-1P5, Bank6 (Hard core) of GW1N-2, and Bank0 of GW1N-9 support MIPI I/O input.
- [2] The LVCMOS12 standard can be implemented with LVCMOS12, LVCMOS12UD15, LVCMOS12UD18, LVCMOS12UD25, and LVCMOS12UD33 I/O types, which support different V_{CCIO}. The same is true for the LVCMOS15/LVCMOS18/LVCMOS25/LVCMOS33 standards.
- [3] OD=over drive, UD=under drive. When using the OD/UD types, you need to set the Pull Mode of the corresponding IO to NONE and the PCI Clamp of the corresponding IO to OFF.

2.3.2 True LVDS Design

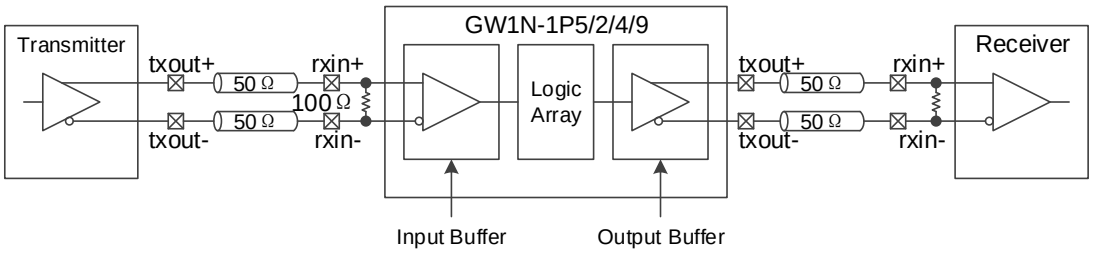
The GW1N series of FPGA products (except GW1N-1) support true LVDS output. In addition, the GW1N series of FPGA products support LVDS25E, MLVDS25E, BLVDS25E, etc.

For more information about true LVDS, see UG174, GW1N-1P5 Pinout, UG171, GW1N-2 Pinout, UG105, GW1N-4 Pinout, and UG114,

GW1N-9 Pinout.

True LVDS input needs a 100Ω termination resistor, see Figure 2-11 for the reference design. Specific banks of the GW1N series of FPGA products support programmable on-chip 100Ω input differential termination resistors, see UG289, Gowin Programable IO User Guide.

Figure 2-11 True LVDS Design



For information about termination for LVDS25E, MLVDS25E, and BLVDS25E, please refer to UG289, Gowin Programmable IO User Guide.

2.3.3 I/O Logic

Figure 2-12 shows the I/O logic input and output of the GW1N series of FPGA products.

Figure 2-12 I/O Logic Input and Output

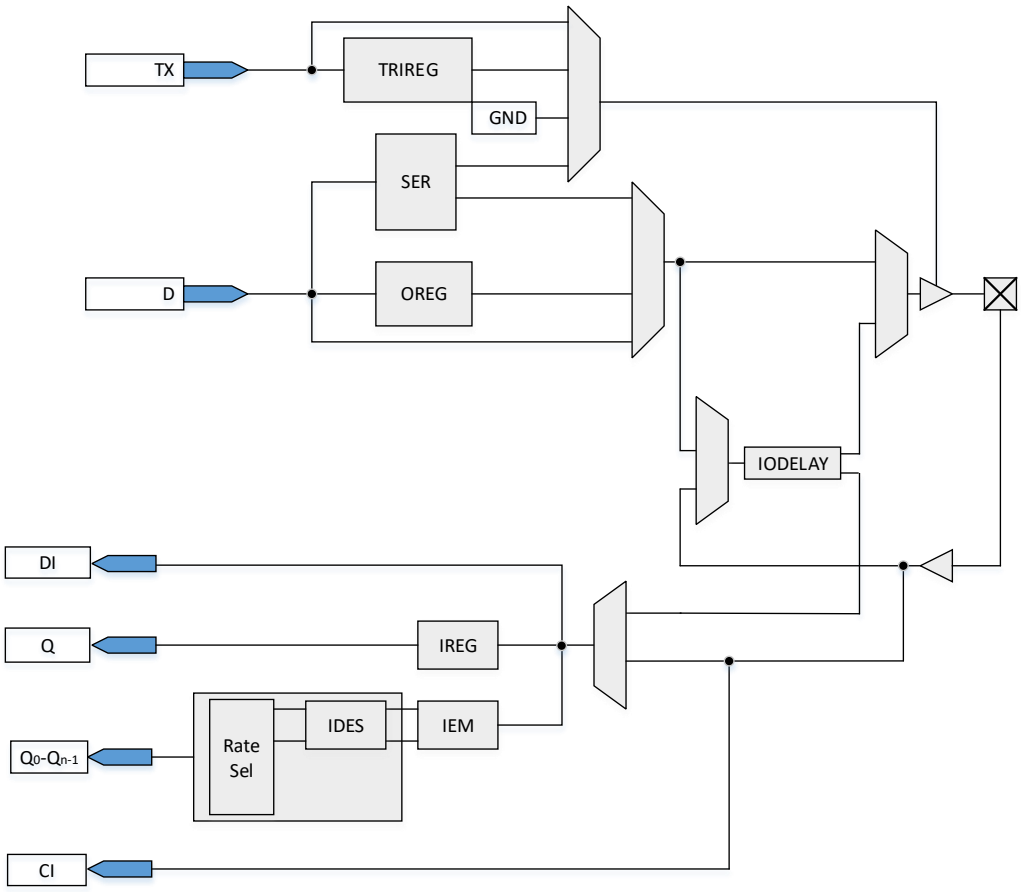


Table 2-3 Port Description

Port	I/O	Description
CI[1]	Input	GCLK input signal. For the number of GCLK input signals, please refer to UG107, GW1N-1 Pinout, UG171, GW1N-2 Pinout, UG174, GW1N-1P5 Pinout, UG105, GW1N-4 Pinout, and UG114, GW1N-9 Pinout.
DI	Input	IO port low-speed input signal input into the fabric directly.
Q	Input	IREG output signal in the SDR module.
Q_0-Q_{n-1}	Input	IDES output signal in the DDR module.

Note!

When CI is used as GCLK input, DI, Q, and Q0-Qn-1 cannot be used as I/O input and output.

Descriptions of the I/O logic modules of the GW1N series of FPGA products are presented below.

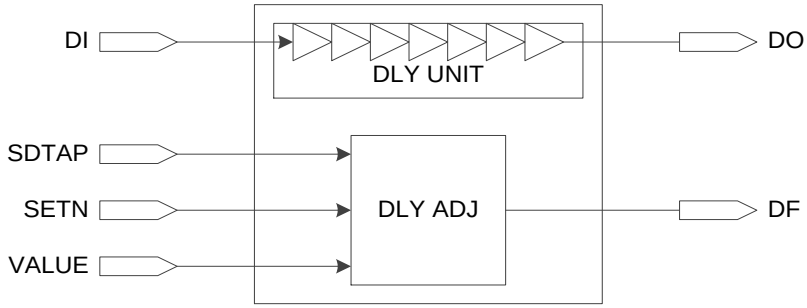
IODELAY

See Figure 2-13 for an overview of the IODELAY module. Each I/O of the GW1N series of FPGA products contains the IODELAY module, through which you can add additional delays to the I/O to adjust the delay of the signal. The delay time of each step is $T_{dlyunit}$, and the number of steps is DLYSTEP. The total delay time of IODELAY can be calculated as follows: $T_{totdly} = T_{dlyoffset} + T_{dlyunit} * DLYSTEP$. See Table 2-4 for the total delay time.

Table 2-4 Total Delay of IODELAY Module

	Min.	Typ.	Max.
$T_{dlyoffset}$	450ps	500ps	550ps
$T_{dlyunit}$	-	30ps	-
DLYSTEP	0	-	127

Figure 2-13 IODELAY Diagram



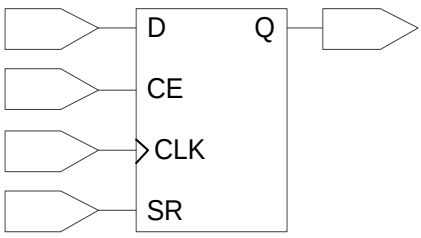
There are two ways to control the delay:

- Static control.
- Dynamic control. The IODELAY module cannot be used for both input and output at the same time

I/O Register

See Figure 2-14 for the I/O register in the GW1N series of FPGA products. Each I/O provides one input register (IREG), one output register (OREG), and one tristate register (TRIREG).

Figure 2-14 I/O Register Diagram



Note!

- CE can be programmed as either active low (0: enable) or active high (1: enable).
- CLK can be programmed as either rising edge triggering or falling edge triggering.

- SR can be programmed as either synchronous/asynchronous SET/RESET or disabled.
- The register can be programmed as a register or a latch.

DES

The GW1N series of FPGA products provide a simple deserializer(DES) for input I/O logic to support advanced I/O protocols.

SER

The GW1N series of FPGA products provide a simple serializer(SER) for output I/O logic to support advanced I/O protocols.

2.3.4 I/O Logic Modes

The I/O Logic of the GW1N series of FPGA products supports several operation modes. In each operation mode, the I/O (or I/O differential pair) can be configured as output, input, INOUT or tristate output (output signal with tristate control).

All pins of GW1N-9 support I/O logic. The pins of GW1N-1(except IOL6(A, B,C….J) and IOR6(A,B,C….J)) support IO logic. The pins of GW1N-4(except IOL10(A, B,C….J) and IOR10(A,B,C….J)) support IO logic. The pins of GW1N-1P5/GW1N-2(except IOT2(A, B), IOT3A) support IO logic.

2.4 Block SRAM

2.4.1 Introduction

The GW1N series of FPGA products provide abundant block SRAM resources. These memory resources are distributed as blocks throughout the FPGA array in the form of rows. Therefore, they are called block static random access memories (BSRAMs). The capacity of each BSRAM can be up to 18,432 bits (18 Kbits). There are four configuration modes: Single Port mode, Dual Port mode, Semi-Dual Port mode, and ROM mode.

An abundance of BSRAM resources provide a guarantee for the user's high-performance design. The features of BSRAMs include:

- Up to 18,432 bits per BSRAM
- Clock frequency up to 190MHz
- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi-Dual Port mode
- Provides parity bits
- Supports ROM Mode
- Data widths from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Byte Enable function for 2-byte and above data widths

- Normal read and write
- Read-before-write
- Write-through

2.4.2 BSRAM Configuration Modes

BSRAMs in the GW1N series of FPGA products support various data widths, see Table 2-5.

Table 2-5 BSRAM Size Configuration[3]

Single Port Mode	Dual Port Mode[1]	Semi-Dual Port Mode	ROM Mode[2]
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

Note!

- [1] For the GW1N-9 devices, only the C version supports dual port mode.
- [2] For the GW1N-4 devices, only the D version supports ROM mode.
- [3] The BSRAM of C version GW1N-9 does not support data widths of 1 bit and 2 bits.

Single Port Mode

The single port mode supports 2 read modes (bypass mode and pipeline mode) and 3 write modes (normal mode, write-through mode, and read-before-write mode). In single port mode, writing to or reading from one port at one clock edge is supported. During the write operation, the written data will be transferred to the output of the BSRAM. When the output register is bypassed, the new data will show up at the same write clock rising edge.

For more information on single port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Dual Port Mode

The dual port mode supports 2 read modes (bypass mode and pipeline mode) and 2 write modes (normal mode and write-through mode).

The applicable operations are as follows:

- Two independent read operations
- Two independent write operations
- An independent read operation and an independent write operation

Note!

Performing read and write operations to the same address at the same time is not allowed.

For more information on dual port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Semi-Dual Port Mode

The semi-dual port mode supports 2 read modes (bypass mode and pipeline mode) and 1 write mode (normal mode). Semi-dual port mode supports simultaneous read and write operations in the form of writing to port A and reading from port B.

Note!

Performing read and write operations to the same address at the same time is not allowed.

For more information on semi-dual port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

ROM Mode

BSRAMs can be configured as ROMs. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization is completed during the device power-on process.

Each BSRAM can be configured as one 16 Kbit ROM. For more information on ROM mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

2.4.3 Mixed Data Width Configuration

The BSRAMs in the GW1N series of FPGA products support mixed data width operations. In dual port and semi-dual port mode, the data widths for read and write can be different, see Table 2-6 and Table 2-7.

Table 2-6 Dual Port Mixed Read/Write Data Width Configuration[1],[2]

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

- [1] For the GW1N-9 devices, only the C version supports dual port mode.
- [2] **"*"** denotes the modes supported.

Table 2-7Semi-dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512x32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*" denotes the modes supported.

2.4.4 Byte-enable

BSRAMs support the byte-enable function. For data longer than a byte, the additional bits can be blocked, allowing only the selected portion to be written into the memory. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB) and byte-enable parameter options can be used to control the BSRAM write operation.

Note!

For the GW1N series, only GW1N-1P5, GW1N-1P5B, GW1N-1P5C, GW1N-2, GW1N-2B, GW1N-2C, and GW1N-4D support the byte-enable function.

2.4.5 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

2.4.6 Synchronous Operation

- All the input registers of BSRAMs support synchronous write.
- The output registers can be used as pipeline registers to improve design performance.
- The output registers are bypass-able.

2.4.7 BSRAM Operation Modes

The BSRAM supports five different operations, including two read modes (Bypass Mode and Pipeline Mode) and three write modes (Normal Mode, Write-Through Mode, and Read-before-Write Mode).

Read Mode

The following two read modes are supported.

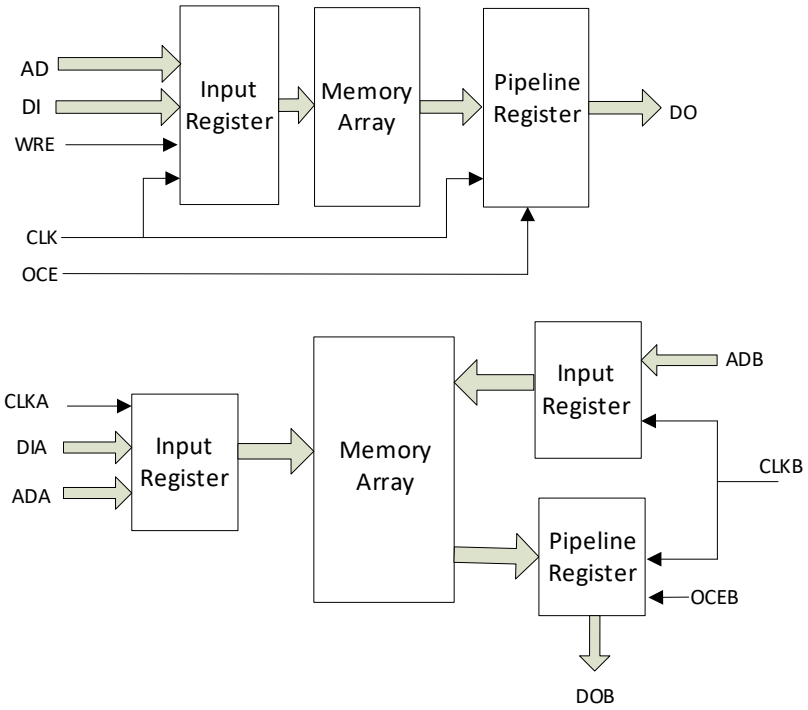
PIPELINE MODE

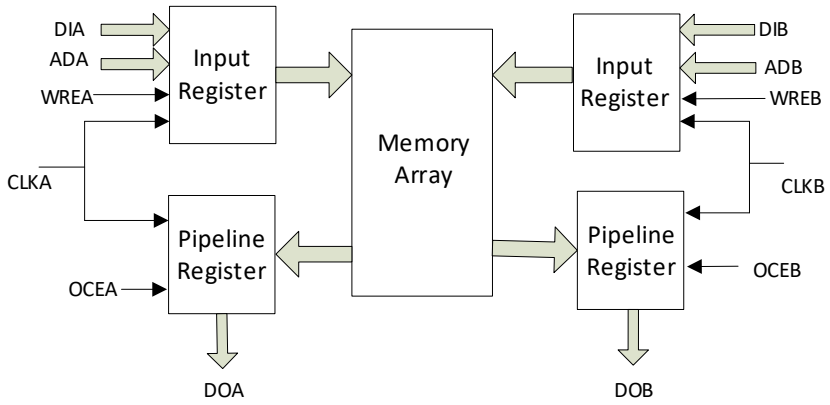
When a synchronous write cycles into a memory array with pipeline registers enabled, the data can be read from pipeline registers in the next clock cycle. The data bus can be up to 36 bits in this mode.

BYPASS MODE

When a synchronous write cycles into a memory array with pipeline registers bypassed, the outputs are registered at the memory array.

Figure 2-15 Pipeline Mode in Single Port Mode, Dual Port Mode, and Semi-dual Port Mode





Write Mode

NORMAL WRITE MODE

In this mode, when you write data to one port, the output data of this port does not change. The written data will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when you write data to one port, the written data will appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when you write data to one port, the written data will be stored in the memory according to the address, and the original data in this address will appear at the output of this port.

2.4.8 Clock Mode

Table 2-8 lists the clock modes in different BSRAM modes:

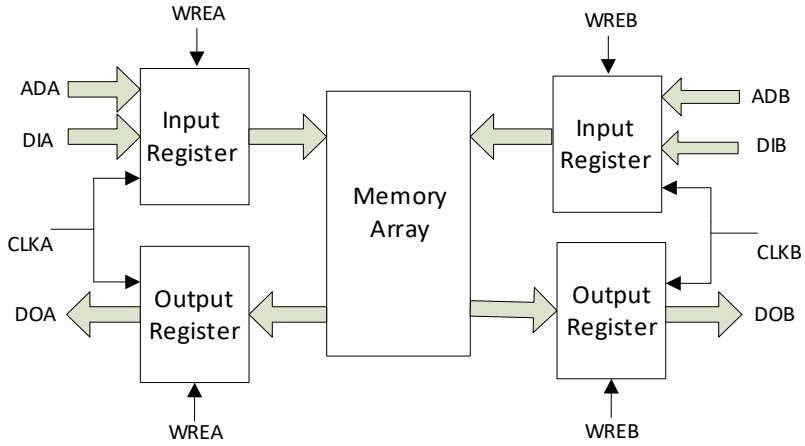
Table 2-8 Clock Modes in Different BSRAM Modes

Clock Mode	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 2-16 shows the independent clocking operations in dual port mode with one clock at each port. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

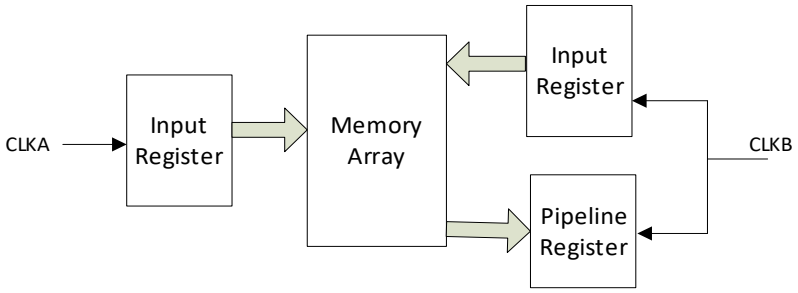
Figure 2-16 Independent Clock Mode



Read/Write Clock Mode

Figure 2-17 shows the read/write clocking operations in semi-dual port mode with one clock at each port. The write clock (CLKA) controls data inputs, write addresses and read/write enable signals of Port A. The read clock (CLKB) controls data outputs, read addresses, and read enable signals of Port B.

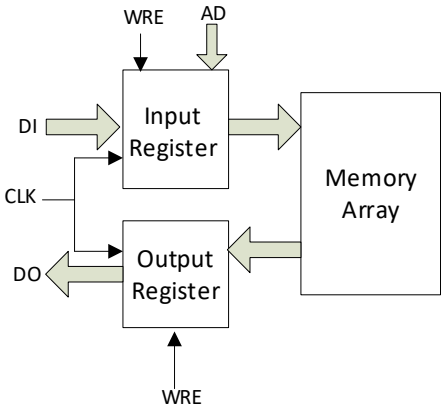
Figure 2-17 Read/Write Clock Mode



Single Port Clock Mode

Figure 2-18 shows the clocking operation in single port mode.

Figure 2-18 Single Port Clock Mode



2.5 User Flash(GW1N-1)

GW1N-1 provides a User Flash with 12 Kbytes (48 pages x 256 bytes). The key features include:

- NOR Flash
- 100,000 write cycles
- Greater than 10 years of data retention at +85℃
- Selectable input/output data widths of 8/16/32 bits
- Page size: 256 bytes
- Standby current: 3μA
- Page write time: 8.2ms

For more information about the User Flash in GW1N-1, please refer to UG295, Gowin User Flash User Guide. For the correspondence between User Flash primitives and devices supported, please refer to Table 3-1 Devices Supported of UG295, Gowin User Flash User Guide.

2.6 User Flash(GW1N-1P5/2/4/9)

GW1N-1P5/2/4/9 provide a User Flash. The capacity of the User Flash in GW1N-1P5/2 is 96 Kbits. The capacity of the User Flash in GW1N-4 is 256 Kbits. The capacity of the User Flash in GW1N-9 is 608 Kbits. The User Flash consists of row memories and column memories. One row memory consists of 64 column memories. The capacity of one column memory is 32 bits, and the capacity of one row memory is 64*32=2048 bits. Page erase is supported, and the capacity of one page is 2048 bytes, that is, one page contains 8 rows. The key features include:

- NOR Flash
- 10,000 write cycles
- Greater than 10 years of data retention at +85℃
- Data width: 32 bits
- Capacity in GW1N-1P5/2 : 48 rows x 64 columns x 32 = 96 Kbits
- Capacity in GW1N-4 : 128 rows x 64 columns x 32 = 256 Kbits
- Capacity in GW1N-9 : 304 rows x 64 columns x 32 = 608 Kbits
- Page erase capability: 2,048 bytes per page
- Fast Page Erase/Word Program Operation
- Clock frequency: 40 MHz
- Word Programming Time: ≤16μs
- Page Erase Time: ≤120ms
- Current
  - Read current/duration: 2.19mA/25ns (V_{CC}) & 0.5mA/25ns (V_{CCX})(MAX)
  - Program/erase operation: 12/12mA(MAX)

For more information about the User Flash in GW1N-1P5/2/4/9,

please refer to UG295, Gowin User Flash User Guide. For the correspondence between User Flash primitives and devices supported, please refer to Table 3-1 Devices Supported of UG295, Gowin User Flash User Guide.

2.7 Digital Signal Processing

GW1N-4/9 provide abundant DSP resources. Gowin's DSP solutions can address high-performance digital signal processing needs such as FIR and FFT designs. The DSP resources have the advantages of stable timing performance, high resource utilization, and low power consumption.

The DSP resources offer the following functions:

- Multipliers with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data widths
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number
- Supports pipeline mode and bypass mode.

2.7.1 Macro

The DSP blocks are distributed throughout the FPGA array in the form of rows. Each DSP block occupies 9 CFU locations. Each DSP block contains two macros, and each macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU.

Pre-adder

Each DSP macro contains two pre-adders for implementing pre-addition, pre-subtraction, and shifting.

The pre-adders are located at the first stage and have two input ports:

- Parallel 18-bit input B or SBI
- Parallel 18-bit input A or SIA

Note!

Each input port supports pipeline mode and bypass mode.

Gowin's pre-adders can be used independently as function blocks, which support 9-bit and 18-bit width.

Multiplier

The multipliers are located after the pre-adders. The multipliers can be configured as 9 x 9, 18 x 18, 36 x 18, or 36 x 36. Register mode and bypass mode are supported in both input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers

- Four 9 x 9 multipliers

Note!

Two macros can form one 36 x 36 multiplier

Arithmetic Logic Unit

Each DSP macro contains one 54-bit ALU, which can further enhance multipliers' functions. Register mode and bypass mode are supported in both input and output ports. The functions include:

- Addition/subtraction operations of multiplier output data/0, data A, and data B.
- Addition/subtraction operations of multiplier output data/0, data B, and carry C.
- Addition/subtraction operations of data A, data B, and carry C.

2.7.2 DSP Operation Modes

- Multiplier mode
- Multiply accumulator mode
- Multiply-add accumulator mode

For more information on the DSP resources, see UG287, Gowin Digital Signal Processing (DSP) User Guide.

2.8 MIPI D-PHY

2.8.1 Hard MIPI D-PHY RX Core(GW1N-2)

GW1N-2 provides a hard MIPI D-PHY RX core that supports the "MIPI Alliance Standard for D-PHY Specification(Version 2.1)". The dedicated D-PHY core supports MIPI DSI and CSI-2 mobile video interfaces for cameras and displays. The key features include:

- High Speed RX at up to 8Gbps per quad(four data lanes)
- Supports up to 4 data lanes and 1 clock lane
- Supports bidirectional low-power (LP) mode at up to 10Mbps per lane
- Supports built-in HS Sync, bit and lane alignment
- Supports MIPI D-PHY RX 1:8 and 1:16 deserialization modes
- Supports MIPI DSI and MIPI CSI-2 link layers
- Available on Bank6

For more information, see *IPUG778, Gowin GW1N-2 Hardened MIPI D-PHY RX User Guide*.

2.8.2 Soft MIPI D-PHY RX/TX Implemented by Using GPIOs

When implementing soft MIPI D-PHY RX/TX with GPIOs, three IO types are available: TLVDS, ELVDS, and MIPI IO.

All GW1N FPGAs support the TLVDS/ELVDS types. To implement MIPI D-PHY with the TLVDS/ELVDS types, you need to emulate MIPI HS

and MIPI LP by using LVDS25(E)+LVCMOS12 and need to add external resistors.

Some GW1N FPGAs support the MIPI IO type. The MIPI IO has an internal resistor network and supports automatic switching between HS and LP. The support list of the MIPI IO type is shown in Table 2-9.

For information on IO type selection and off-chip termination, please refer to “4 Functional Description” in *IPUG948, Gowin MIPI D-PHY RX TX Advance User Guide*.

Table 2-9 List of GW1N series of FPGA Products that Support MIPI IO Type

MIPI Input/Output	GW1N-1P5	GW1N-2	GW1N-9
MIPI Input	Bank2(with dynamic ODT)	Bank2(with dynamic ODT)	Bank0(with dynamic ODT)
MIPI Output	Bank0/3/4/5(with dynamic ODT)	Bank0/3/4/5(with dynamic ODT)	Bank2

The key features of the soft MIPI D-PHY RX/TX include:

- MIPI Alliance Standard for D-PHY Specification, Version 1.2
- High Speed RX and TX at up to 4.8Gbps
- Supports up to 4 data lanes and 1 clock lane
- Supports multiple PHYs(if there are enough IOs available)
- Supports bidirectional low-power (LP) mode
- Supports MIPI DSI and MIPI CSI-2 link layers
- Supports built-in HS Sync, bit and lane alignment
- Supports MIPI D-PHY RX 1:8 and 1:16 deserialization modes
- Supports IO Types of ELVDS, TLVDS, MIPI IO, etc.
- Bank0/2 of GW1N-9 support I3C

For more information, see IPUG948, Gowin MIPI D-PHY RX TX Advance User Guide.

2.9 Clocks

The clock resources and wiring are critical for high-performance applications in FPGA. The GW1N series of FPGA products provide global clocks (GCLKs) which connect to all the registers directly. In addition, high-speed clocks (HCLKs), PLLs, etc. are provided.

For more information on the GCLKs, HCLKs, PLLs, see UG286, Gowin Clock User Guide.

2.9.1 Global Clocks

The Global Clock(GCLK) resources are distributed as quadrants in the GW1N devices, with each quadrant providing eight GCLKs. The clock sources of GCLKs include dedicated clock input pins and CRUs, and

better clock performance can be achieved by using the dedicated clock input pins.

2.9.2 PLLs

The PLL (Phase-locked Loop) is a feedback control circuit. The frequency and phase of the internal oscillator signal are controlled by the external input reference clock.

PLLs in the GW1N series of FPGA products can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

2.9.3 High-speed Clocks

The high-speed clocks (HCLKs) are designed to facilitate high-performance I/O data transmission and are specifically tailored for source synchronous data transmission protocols, see Figure 2-19 - Figure 2-22.

Figure 2-19 GW1N-1 HCLK Distribution

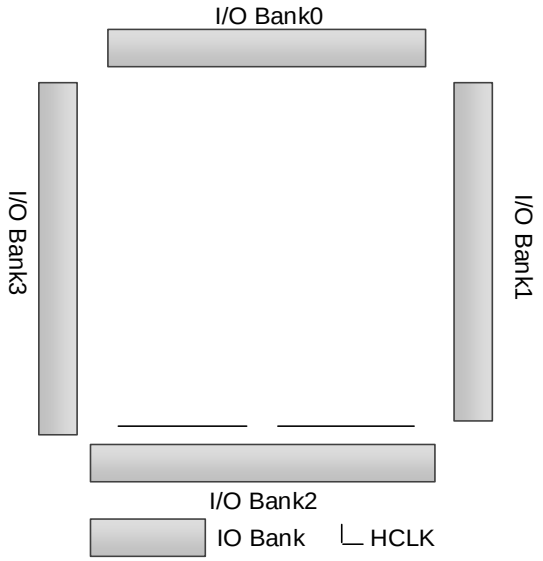


Figure 2-20 GW1N-1P5/2 HCLK Distribution

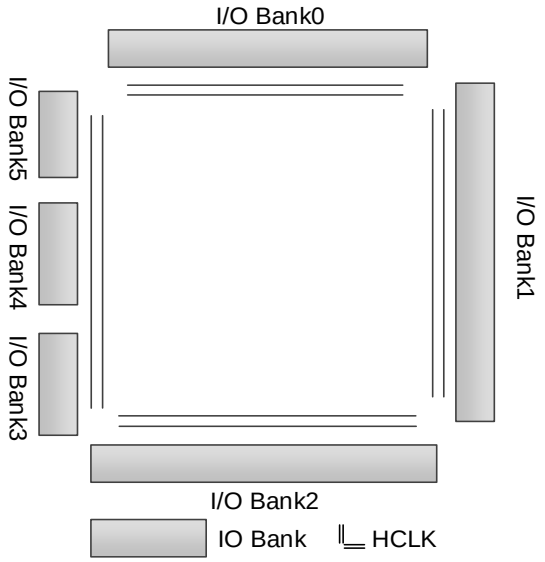


Figure 2-21 GW1N-4 HCLK Distribution

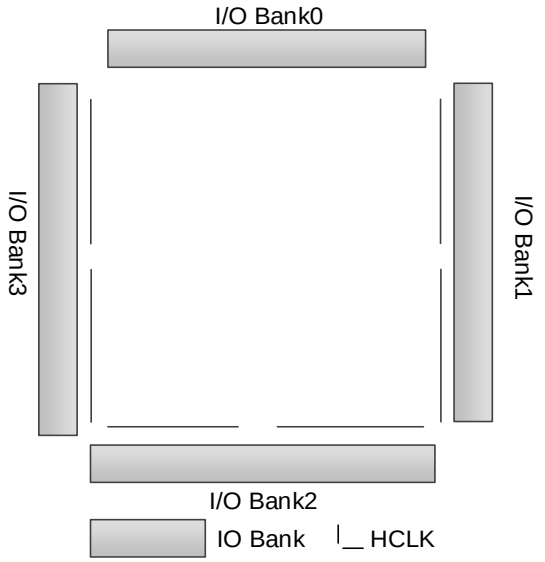
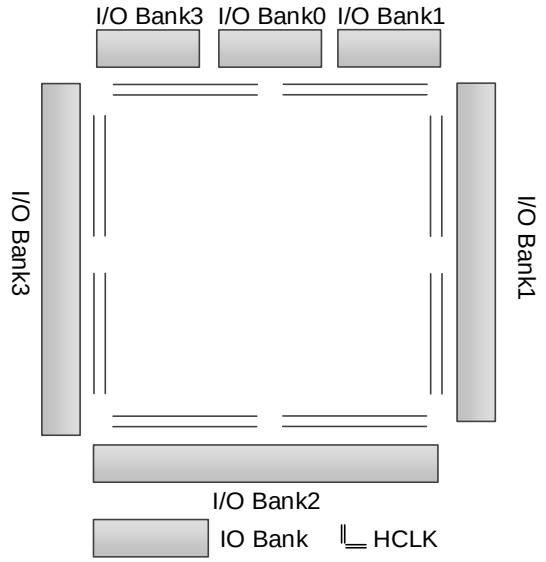


Figure 2-22 GW1N-9 HCLK Distribution



2.10 Long Wires

As a supplement to the CRU, the GW1N series of FPGA products provide another kind of routing resource - the long wire, which can be used for clock, clock enable, set/reset, or other high fan out signals.

2.11 Global Set/Reset

The GW1N series of FPGA products offer a dedicated global set/reset (GSR) network that connects directly to the device's internal logic and can be used as asynchronous/synchronous set or asynchronous/synchronous reset, with the registers in the CFUs and I/Os being able to be configured independently.

2.12 Programming & Configuration

The GW1N series of FPGA products support SRAM configuration and Flash programming. Flash programming includes on-chip Flash programming and off-chip Flash programming. The GW1N series of FPGA products support DUAL BOOT, allowing you to back up data to the off-chip Flash as needed.

Besides JTAG, the GW1N series of FPGA products also support Gowin’s own GowinCONFIG configuration mode: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, CPU, and I2C Slave. All the devices support JTAG and AUTO BOOT.

For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

SRAM Configuration

If SRAM configuration is used, the configuration data needs to be re-downloaded after each power-up.

Flash Programming

The Flash programming data is stored in the on-chip Flash. Each time the device is powered up, the configuration data is transferred from the Flash to the SRAM. Configuration can be completed within a few milliseconds after power-up, which is also known as "instant on".

The GW1N series of FPGA products (except the GW1N-4 A version) support the feature of background upgrade. That is to say, you can program the on-chip Flash or off-chip Flash via the JTAG[1] interface without affecting the current working state. During programming, the device works according to the previous configuration. After the programming is done, you can trigger RECONFIG_N with a low level to complete the upgrade. This feature is suitable for the applications requiring long online time and irregular upgrades.

Note!

- [1] GW1N-1P5 and GW1N-2 can support the I^2C background upgrade by using the goConfig I2C IP. It is recommended to use the JTAG interface to implement the background upgrade.
- [2] As a configuration pin, RECONFIG_N is an input pin with internal weak pull-up, but as a GPIO, RECONFIG_N can only be used for output. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

In addition, the GW1N series of FPGA products support off-chip Flash programming and DUAL BOOT. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

2.13 On-chip Oscillator

The GW1N series of FPGA products features an on-chip oscillator (with an optimal tolerance of ±5%). This on-chip oscillator provides a programmable user clock and serves as a clock source for the MSPI configuration mode during the configuration process.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters.

The following formula is used to get the output clock frequency of the on-chip oscillator of GW1N-1:

$$f_{out}=240MHz/Param.$$

The following formula is used to get the output clock frequency of the on-chip oscillator of GW1N-1P5/2/9:

$$f_{out}=250MHz/Param.$$

The following formula is used to get the output clock frequency of the on-chip oscillator of GW1N-4:

$$f_{out}=210MHz/Param.$$

Note!

“Param” should be even numbers from 2 to 128.

Table 2-10, Table 2-11, and Table 2-12 list some frequencies provided by the on-chip crystal oscillator.

Table 2-10 Output Frequency Options of the On-chip Oscillator of GW1N-4

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.1MHz[1]	8	6.6MHz	16	13.1MHz
1	4.6MHz	9	7MHz	17	15MHz
2	4.8MHz	10	7.5MHz	18	17.5MHz
3	5MHz	11	8.1MHz	19	21MHz
4	5.3MHz	12	8.8MHz	20	26.3MHz
5	5.5MHz	13	9.5MHz	21	35MHz
6	5.8MHz	14	10.5MHz	22	52.5MHz
7	6.2MHz	15	11.7MHz	23	105MHz[2]

Table 2-11 Output Frequency Options of the On-chip Oscillator of GW1N-1P5/2/9

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz[1]	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz[2]

Table 2-12 Output Frequency Options of the On-chip Oscillator of GW1N-1

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.4MHz[1]	8	7.5MHz	16	15MHz
1	5.2MHz	9	8MHz	17	17MHz
2	5.5MHz	10	8.6MHz	18	20MHz
3	5.7MHz	11	9MHz	19	24MHz
4	6MHz	12	10MHz	20	20MHz

Mode	Frequency	Mode	Frequency	Mode	Frequency
5	6.3MHz	13	11MHz	21	40MHz
6	6.7MHz	14	12MHz	22	60MHz
7	7MHz	15	13MHz	23	120MHz[2]

Note!

- [1] Default frequency.
- [2] This is not available for the MSPI configuration mode.

3 DC and Switching Characteristics

Note!

Please ensure that you use Gowin's devices within the recommended operating conditions and ranges. Data beyond the working conditions and ranges are for reference only. Gowin does not guarantee that all devices will operate normally beyond the operating conditions and ranges.

3.1 Operating Conditions

3.1.1 Absolute Max. Ratings

Table 3-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	Core voltage(LV version)	-0.5V	1.32V
	Core voltage(UV version)	-0.5V	3.75V
V_{CCIO}	I/O Bank voltage	-0.5V	3.75V
V_{CCX}	Auxiliary voltage	-0.5V	3.75V
V_{CCD}	Hard-core MIPI D-PHY core voltage(GW1N-2)	-0.5V	1.32V
V_{CCIOD}	Hard-core MIPI D-PHY I/O voltage(GW1N-2)	-0.5V	1.32V
-	I/O voltage applied[1]	-0.5V	3.75V
Storage Temperature	Storage Temperature	-65℃	+150℃
Junction Temperature	Junction Temperature	-40℃	+125℃

Note!

[1] Overshoot and undershoot of -2V to (V_{IHMAX} + 2)V are allowed for a duration of <20 ns.

3.1.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V_{CC}	Core voltage(LV version)	1.14V	1.26V
	Core voltage(UV version)	1.71V	3.6V
V_{CCIO}	I/O Bank voltage	1.14V	3.6V
V_{CCX}	Auxiliary voltage(GW1N-4/9)	2.375V	3.6V
	Auxiliary voltage(GW1N-1P5/2)	1.71V	3.6V
V_{CCD}[1]	Hard MIPI D-PHY core voltage(GW1N-2)	1.14V	1.26V
V_{CCIOD}[1]	Hard MIPI D-PHY I/O voltage(GW1N-2)	1.14V	1.26V
T_{JCOM}	Junction temperature for commercial operations	0℃	+85℃
T_{JIND}	Junction temperature for industrial operations	-40℃	+100℃

Note!

- [1] If the hard MIPI D-PHY is not used, you can leave the V_{CCD} and V_{CCIOD} pins floating, or connect them to a 1.2V supply.
- For some packages, V_{CCIO} and V_{CCX} may share the same pin. In this case, V_{CCX} requirements must be met first.
- The allowable ripples on V_{CC}, V_{CCIO}, and V_{CCX} are 3%, 5%, and 5% respectively. For devices of which the PLL is powered directly with V_{CC}, the ripple on V_{CC} can affect the jitter characteristics of the PLL output clock; 2). The ripple on V_{CCIO} can eventually be passed on to the output waveform of the IO Buffer.
- For more information on the power supplies, please refer to UG107, GW1N-1 Pinout, UG171, GW1N-2 Pinout, UG174, GW1N-1P5 Pinout, UG105, GW1N-4 Pinout, and UG114, GW1N-9 Pinout.

3.1.3 Power Supply Ramp Rates

Table 3-3 Power Supply Ramp Rates

Name	Description	Device	Min.	Typ.	Max.
V_{CC} Ramp	Power supply ramp rates for V_{CC}	GW1N-1	1.2mV/μs	-	40mV/μs
		GW1N- 1P5/2/4/9	0.6mV/μs	-	6mV/μs
V_{CCX} Ramp	Power supply ramp rates for V_{CCX}	GW1N	0.6mV/μs	-	10mV/us
V_{CCIO} Ramp	Power supply ramp rates for V_{CCIO}	GW1N	0.1mV/μs	-	10mV/us

Note!

- A monotonic ramp is required for all power supplies.

- All power supplies need to be in the operating range as defined in Table 3-2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

3.1.4 Hot Socketing Specifications

Table 3-4 Hot Socketing Specifications

Name	Description	Condition	I/O Type	Max.
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	I/O	150uA
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	TDI, TDO, TMS,TCK	120uA

3.1.5 POR Specifications

Table 3-5 POR Parameters

Name	Description	Device	Name	Value
V_{POR_UP}	Power on reset ramp up trip point	GW1N-1	V_{CC}	0.75V
			V_{CCIO}	0.85V
		GW1N-1P5, GW1N-2	V_{CC}	0.8V
			V_{CCX}	1.5V
			V_{CCIO}	0.95V
		GW1N-4	V_{CC}	0.95V
			V_{CCX}	1.95V
			V_{CCIO}	0.95V
		GW1N-9	V_{CC}	0.95V
			V_{CCX}	1.95V
			V_{CCIO}	0.95V
V_{POR_DOWN}	Power on reset ramp down trip point	GW1N-1	V_{CC}	TBD
			V_{CCIO}	TBD
		GW1N-1P5, GW1N-2	V_{CC}	0.65V
			V_{CCX}	1.3V
			V_{CCIO}	0.75V
		GW1N-4	V_{CC}	0.75V

Name	Description	Device	Name	Value
			V_{CCX}	1.8V
			V_{CCIO}	0.6V
		GW1N-9	V_{CC}	0.75V
			V_{CCX}	1.8V
			V_{CCIO}	0.6V

3.2 ESD performance

Table 3-6 GW1N ESD - HBM

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
CS100H	-	-	HBM>1,000 V	-	-
CS30	HBM>1,000 V	-	-	-	-
CS42	-	-	HBM>1,000 V	-	-
CS42H	-	-	HBM>1,000 V	-	-
CS72	-	-	-	HBM>1,000 V	-
EQ144	-	-	HBM>1,000 V	HBM>1,000 V	HBM>1,000 V
EQ176	-	-	-	-	HBM>1,000 V
FN32	-	-	-	-	-
LQ100	-	HBM>1,000 V	HBM>1,000 V	HBM>1,000 V	HBM>1,000 V
LQ100X	-	HBM>1,000 V	HBM>1,000 V	-	-
LQ144	-	-	-	HBM>1,000 V	HBM>1,000 V
LQ144F	-	-	HBM>1,000 V	-	-

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
LQ144X	-	-	HBM>1,000 V	-	-
LQ176	-	-	-	-	HBM>1,000 V
MG100	-	-	-	-	HBM>1,000 V
MG100T	-	-	-	-	HBM>1,000 V
MG121	-	-	HBM>1,000 V	-	-
MG121X	-	-	HBM>1,000 V	-	-
MG132	-	-	HBM>1,000 V	-	-
MG132H	-	-	HBM>1,000 V	-	-
MG132X	-	-	HBM>1,000 V	HBM>1,000 V	-
MG160	-	-	-	HBM>1,000 V	HBM>1,000 V
MG196	-	-	-	-	HBM>1,000 V
MG49	-	-	HBM>1,000 V	-	-
PG256	-	-	-	HBM>1,000 V	HBM>1,000 V
PG256M	-	-	-	HBM>1,000 V	-
QN32	-	-	HBM>1,000 V	HBM>1,000 V	-
QN32X	-	-	HBM>1,000 V	-	-
QN48	-	-	HBM>1,000 V	HBM>1,000 V	HBM>1,000 V
QN48F	-	-	-	-	HBM>1,000 V

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
QN48H	-	-	HBM>1,000 V	-	-
QN48X	-	HBM>1,000 V	-	-	-
QN48XF	-	HBM>1,000 V	-	-	-
QN60	-	-	-	-	HBM>1,000 V
QN88	-	-	HBM>1,000 V	HBM>1,000 V	HBM>1,000 V
UG169	-	-	-	HBM>1,000 V	HBM>1,000 V
UG256	-	-	-	-	HBM>1,000 V
UG332	-	-	-	-	HBM>1,000 V

Table 3-7 GW1N ESD - CDM

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
CS100H	-	-	CDM>500V	-	-
CS30	CDM>500V	-	-	-	-
CS42	-	-	CDM>500V	-	-
CS42H	-	-	CDM>500V	-	-
CS72	-		-	CDM>500V	-
EQ144	-	-	-	CDM>500V	CDM>500V
EQ176	-	-	-	-	CDM>500V
FN32	-	-	-	-	-
LQ100	-	-	CDM>500V	CDM>500V	CDM>500V
LQ100X	-	CDM>500V	CDM>500V	-	-
LQ144	-	-	CDM>500V	CDM>500V	CDM>500V
LQ144F	-	-	CDM>500V	-	-
LQ144X	-	-	CDM>500V	-	-

Device	GW1N-1	GW1N-1P5	GW1N-2	GW1N-4	GW1N-9
LQ176	-	-	-	-	CDM>500V
MG100	-	-	-	-	CDM>500V
MG100T		-	-	-	-
MG121	-	-	CDM>500V	-	-
MG121X	-	-	CDM>500V	-	-
MG132	-	-	CDM>500V	-	-
MG132H			CDM>500V		
MG132X	-	-	CDM>500V	CDM>500V	-
MG160	-	-	-	CDM>500V	CDM>500V
MG196	-	-	-	-	CDM>500V
MG49	-	-	CDM>500V	-	-
PG256	-	-	-	CDM>500V	CDM>500V
PG256M	-	-	-	CDM>500V	-
QN32	-	-	CDM>500V	CDM>500V	-
QN32X	-	-	CDM>500V	-	-
QN48	-	-	CDM>500V	CDM>500V	CDM>500V
QN48F	-	-	-	-	CDM>500V
QN48H	-	-	CDM>500V	-	-
QN48X	-	CDM>500V	-	-	-
QN48XF	-	CDM>500V	-	-	-
QN60	-	-	-	-	CDM>500V
QN88	-	-	CDM>500V	CDM>500V	CDM>500V
UG169		-		CDM>500V	CDM>500V
UG256	-	-	-	-	CDM>500V
UG332	-	-	-	-	CDM>500V

3.3 DC Electrical Characteristics

3.3.1 DC Electrical Characteristics over Recommended Operating Conditions

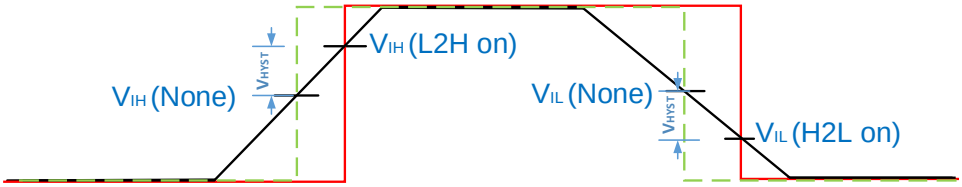
Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCIO}<V_{IN}<V_{IH}$(MAX)	-	-	210μA
		$0<V_{IN}<V_{CCIO}$	-	-	10μA
I_{PU}	I/O Active Pull-up Current(I/O Active Pull-up Current)	$0<V_{IN}<0.7V_{CCIO}$	-30μA	-	-150μA
I_{PD}	I/O Active Pull-down Current(I/O Active Pull-down Current)	V_{IL}(MAX)$<V_{IN}<V_{CCIO}$	30μA	-	150μA
I_{BHLS}	Bus Hold Low Sustaining Current(Bus Hold Low Sustaining Current)	$V_{IN}=V_{IL}$(MAX)	30μA	-	-
I_{BHHS}	Bus Hold High Sustaining Current(Bus Hold High Sustaining Current)	$V_{IN}=0.7V_{CCIO}$	-30μA	-	-
I_{BHLO}	Bus Hold Low Overdrive Current(Bus Hold Low Overdrive Current)	$0\le V_{IN}\le V_{CCIO}$	-	-	150μA
I_{BHHO}	Bus Hold High Overdrive Current	$0\le V_{IN}\le V_{CCIO}$	-	-	-150μA
V_{BHT}	Bus Hold Trip Points		V_{IL}(MAX)	-	V_{IH}(MIN)
C1	I/O Capacitance(I/O Capacitance)			5pF	8pF
V_{HYST}	Hysteresis for Schmitt Trigger inputs	V_{CCIO}=3.3V, Hysteresis=L2H[1],[2]	-	200mV	-
		V_{CCIO}=2.5V, Hysteresis= L2H	-	125mV	-
		V_{CCIO}=1.8V, Hysteresis= L2H	-	60mV	-

Name	Description	Condition	Min.	Typ.	Max.
		V_{CCIO}=1.5V, Hysteresis= L2H	-	40mV	-
		V_{CCIO}=1.2V, Hysteresis= L2H	-	20mV	-
		V_{CCIO}=3.3V, Hysteresis= H2L[1],[2]	-	200mV	-
		V_{CCIO}=2.5V, Hysteresis= H2L	-	125mV	-
		V_{CCIO}=1.8V, Hysteresis= H2L	-	60mV	-
		V_{CCIO}=1.5V, Hysteresis= H2L	-	40mV	-
		V_{CCIO}=1.2V, Hysteresis= H2L	-	20mV	-
		V_{CCIO}=3.3V, Hysteresis= HIGH[1],[2]	-	400mV	-
		V_{CCIO}=2.5V, Hysteresis= HIGH	-	250mV	-
		V_{CCIO}=1.8V, Hysteresis= HIGH	-	120mV	-
		V_{CCIO}=1.5V, Hysteresis= HIGH	-	80mV	-
		V_{CCIO}=1.2V, Hysteresis= HIGH	-	40mV	-

Note!

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see SUG1541, Gowin Software Physical Constraints User Guide.
- [2] Enabling the L2H (low to high) option means raising V_{IH} by V_{HYST}; enabling the H2L (high to low) option means lowering V_{IL} by V_{HYST}; enabling the HIGH option means enabling both L2H and H2L options, i.e. V_{HYST}(HIGH) = V_{HYST}(L2H) + V_{HYST}(H2L). The diagram is shown below.



3.3.2 Static Current

Table 3-9 Static Current

Device	Name	Description	Device type	C7/I6	C6/I5	C5/I4	Unit
GW1N-1	I_{CC}	V_{CC} current (V_{CC}=1.2V)	LV	2.5	1.8	1.5	mA
	I_{CCIO}	V_{CCIO} current (V_{CCIO}=2.5V)	LV	1	0.8	0.6	mA
GW1N-2	I_{CC} + I_{CCX}	V_{CCX} current and V_{CC} current(V_{CCX}=V_{CC}=3.3V)	UV	15	12	10	mA
	I_{CCIO}	V_{CCIO} current (V_{CCIO}=2.5V)	UV	1.2	1	0.8	mA
	I_{CC}	V_{CC} current (V_{CC}=1.2V)	LV	3	2.5	2.2	mA
	I_{CCX}	V_{CCX} current (V_{CCX}=3.3V)	LV	1.5	0.75	0.6	mA

Device	Name	Description	Device type	C7/I6	C6/I5	C5/I4	Unit
	I_{CCIO}	V_{CCIO} current (V_{CCIO}=2.5V)	LV	0.6	0.5	0.4	mA
GW1N-1P5	I_{CC} + I_{CCX}	V_{CCX} current and V_{CC} current(V_{CCX}=V_{CC}=3.3V)	UV	15	12	10	mA
	I_{CCIO}	V_{CCIO} current (V_{CCIO}=2.5V)	UV	1.2	1	0.8	mA
	I_{CC}	V_{CC} current (V_{CC}=1.2V)	LV	3	2.5	2.2	mA
	I_{CCX}	V_{CCX} current (V_{CCX}=3.3V)	LV	1.5	0.75	0.6	mA
	I_{CCIO}	V_{CCIO} current (V_{CCIO}=2.5V)	LV	0.6	0.5	0.4	mA
GW1N-4	I_{CC}	V_{CC} current (V_{CC}=1.2V)	LV	-	2.8	2.4	mA
	I_{CC}	V_{CC} current (V_{CC}=3.3V)	UV	-	18	16	mA
	I_{CCX}	V_{CCX} current (V_{CCX}=3.3V)	LV/UV	-	0.9	0.7	mA
	I_{CCIO}	V_{CCIO} current (V_{CCIO}=2.5V)	LV/UV	-	0.55	0.4	mA
	I_{CC}	V_{CC} current (V_{CC}=1.2V)	LV(CS72)	-	2.15	1.9	mA
	I_{CCX}	V_{CCX} current (V_{CCX}=2.5V)	LV(CS72)	-	0.89	0.68	mA
	I_{CCIO}	V_{CCIO} current (V_{CCIO}=1.8V)	LV(CS72)	-	0.16	0.13	mA
GW1N-9	I_{CC}	V_{CC} current (V_{CC}=1.2V)	LV	2.8	2.4	2	mA
	I_{CC}	V_{CC} current (V_{CC}=3.3V)	UV	20	18	16	mA
	I_{CCX}	V_{CCX} current (V_{CCX}=3.3V)	LV/UV	1.5	1.3	1	mA
	I_{CCIO}	V_{CCIO} current (V_{CCIO}=2.5V)	LV/UV	0.9	0.7	0.5	mA

Note!

The values in Table 3-9 are typical values at 25℃.

3.3.3 Programming Current

Table 3-10 Programming Current

Device	Description	Device type	Max.(mA)
GW1N-1	V_{CC} current when programming the Flash (V_{CC}=1.2V)	LV	4.8
	V_{CCIO} current when programming the Flash (V_{CCIO}=2.5V)	LV	2.8
GW1N-2	V_{CC} current when programming the Flash (V_{CC}=1.2V)	LV	2.19
	V_{CCX} current when programming the Flash (V_{CC}=3.3V)	LV	12
	V_{CCIO} current when programming the Flash (V_{CCIO}=2.5V)	LV	2
GW1N-1P5	V_{CC} current when programming the Flash (V_{CC}=1.2V)	LV	2.19
	V_{CCX} current when programming the Flash (V_{CC}=3.3V)	LV	12
	V_{CCIO} current when programming the Flash (V_{CCIO}=2.5V)	LV	2
GW1N-4	V_{CC} current when programming the Flash (V_{CC}=1.2V)	LV	2.19
	V_{CCX} current when programming the Flash (V_{CC}=3.3V)	LV	12

Device	Description	Device type	Max.(mA)
	V_{CCIO} current when programming the Flash (V_{CCIO}=2.5V)	LV	2
GW1N-9	V_{CC} current when programming the Flash (V_{CC}=1.2V)	LV	2.19
	V_{CCX} current when programming the Flash (V_{CC}=3.3V)	LV	12
	V_{CCIO} current when programming the Flash (V_{CCIO}=2.5V)	LV	2

Note!

The current values in Table 3-10 are the maximum programming currents at room temperature under normal atmospheric pressure.

3.3.4 Recommended I/O Operating Conditions

Table 3-11 Recommended I/O Operating Conditions

Name	V_{CCIO} (V) for Output			V_{REF} (V) for Input		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.6	-	-	-
LVCMOS33	3.135	3.3	3.6	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.6	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.6	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.6	-	-	-

Name	V_{CCIO} (V) for Output			V_{REF} (V) for Input		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVPECL33E	3.135	3.3	3.6	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.6	-	-	-
SSTL33D_II	3.135	3.3	3.6	-	-	-
HSTL15D	1.425	1.5	1.575	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

3.3.5 Single-ended I/O DC Characteristics

Table 3-12 Single-ended I/O DC Characteristics

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24[2]	-24[2]
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35*V_{CCIO}	0.65*V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35*V_{CCIO}	0.65*V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35*V_{CCIO}	0.65*V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4 or 2[3]	-4 or -2[3]
							8 or 6[3]	-8 or -6[3]
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3*V_{CCIO}	0.5*V_{CCIO}	3.6V	0.1*V_{CCIO}	0.9*V_{CCIO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCIO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCIO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

Note!

- [1] The total DC current limit(sourced and sunk current) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.
- [2] GW1N-1P5 and GW1N-2 do not support 24mA.
- [3] GW1N-1P5/2 support 2mA/6mA, and GW1N-1/4/9 support 4mA/8mA.

3.3.6 Differential I/O DC Characteristics

Table 3-13 Differential I/O DC Characteristics

Name	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage		0	-	2.15	V
V_{CM}	Input Common Mode Voltage(Input Common Mode Voltage)	Half the Sum of the Two Inputs	0.05	-	2.1	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	±100	-	±600	mV
I_{IN}	Input Current	Power On or Power Off	-	-	±20	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T=100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T=100Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between High and Low		-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	-	-	15	mA

3.4 Switching Characteristics

3.4.1 CFU Switching Characteristics

Table 3-14 CFU Internal Timing Parameters[1, 2]

Device	Name	Description	C7/I6		C6/I5		C5/I4		Unit
			Min	Max	Min	Max	Min	Max	
GW1N-1	t_{LUT4_CFU}	LUT4 delay	0.412	0.594	0.556	0.802	0.695	1.002	ns
	t_{SR_CFU}	Set/Reset to Register output	0.648	1.268	0.875	1.712	1.094	2.140	ns
	t_{CO_CFU}	Clock to Register output	0.247	0.340	0.333	0.458	0.417	0.573	ns
GW1N-2/GW1N-1P5	t_{LUT4_CFU}	LUT4 delay	0.412	0.594	0.556	0.802	0.695	1.002	ns
	t_{SR_CFU}	Set/Reset to Register output	0.648	1.268	0.875	1.712	1.094	2.140	ns
	t_{CO_CFU}	Clock to Register output	0.247	0.340	0.333	0.458	0.417	0.573	ns
GW1N-4	t_{LUT4_CFU}	LUT4 delay	-	-	0.492	1.443	TBD	TBD	ns
	t_{SR_CFU}	Set/Reset to Register output	-	-	0.875	1.712	1.094	2.140	ns
	t_{CO_CFU}	Clock to Register output	-	-	0.333	0.458	0.417	0.573	ns
GW1N-9	t_{LUT4_CFU}	LUT4 delay	0.363	0.443	0.556	0.802	0.695	1.002	ns
	t_{SR_CFU}	Set/Reset to Register output	0.648	1.268	0.875	1.712	1.094	2.140	ns
	t_{CO_CFU}	Clock to Register output	0.247	0.340	0.333	0.458	0.417	0.573	ns

Note!

- [1] The min/max values are based on the rising edge delay.
- [2] The LUT4 delay values are based on the delay of input port I3->F.

3.4.2 BSRAM Switching Characteristics

Table 3-15 BSRAM Timing Parameters

Device	Name	Description	C7/I6		C6/I5		C5/I4		Unit
			Min	Max	Min	Max	Min	Max	
GW1N-1	t_{COAD_BSRAM}	Clock to output time of read address/data	2.564	2.564	3.460	3.460	4.325	4.325	ns
	t_{COOR_BSRAM}	Clock to output time of output register	0.613	0.613	0.827	0.827	1.034	1.034	ns
GW1N-2/ GW1N-1P5	t_{COAD_BSRAM}	Clock to output time of read address/data	2.564	2.564	3.460	3.460	4.325	4.325	ns
	t_{COOR_BSRAM}	Clock to output time of output register	0.613	0.613	0.827	0.827	1.034	1.034	ns
GW1N-4	t_{COAD_BSRAM}	Clock to output time of read address/data	-	-	3.460	3.460	4.325	4.325	ns
	t_{COOR_BSRAM}	Clock to output time of output register	-	-	0.827	0.827	1.034	1.034	ns
GW1N-9	t_{COAD_BSRAM}	Clock to output time of read address/data	2.564	2.564	3.460	3.460	4.325	4.325	ns
	t_{COOR_BSRAM}	Clock to output time of output register	0.613	0.613	0.827	0.827	1.034	1.034	ns

Note!

t_{COAD_BSRAM} values refer to the delays in bypass mode.

3.4.3 DSP Switching Characteristics

Table 3-16 DSP Timing Parameters

Device	Name	Description	C7/I6		C6/I5		C5/I4		Unit
			Min	Max	Min	Max	Min	Max	
GW1N-4	t_{COIR_DSP}	Clock to output time of input register	-	-	0.295	0.318	0.369	0.398	ns
	t_{COPR_DSP}	Clock to output time of pipeline register	-	-	0.085	0.101	0.106	0.127	ns

Device	Name	Description	C7/I6		C6/I5		C5/I4		Unit
			Min	Max	Min	Max	Min	Max	
	t_{COOR_DSP}	Clock to output time of output register	-	-	0.046	0.052	0.057	0.065	ns
GW1N-9	t_{COIR_DSP}	Clock to output time of input register	0.219	0.239	0.295	0.318	0.369	0.398	ns
	t_{COPR_DSP}	Clock to output time of pipeline register	0.063	0.075	0.085	0.101	0.106	0.127	ns
	t_{COOR_DSP}	Clock to output time of output register	0.034	0.038	0.046	0.052	0.057	0.065	ns

3.4.4 Gearbox Switching Characteristics

Table 3-17 Gearbox Timing Parameters

Device	Name	Description	C7/I6		C6/I5		C5/I4		Unit
			Min	Max	Min	Max	Min	Max	
GW1N-1/4/9	$FMAX_{IDDR}$	1:2 Gearbox maximum serial input rate	-	400	-	350	-	300	Mbps
	$FMAX_{IDES4}$	1:4 Gearbox maximum serial input rate	-	800	-	750	-	700	Mbps
	$FMAX_{IDES7}$	1:7 Gearbox maximum serial input rate	-	1000	-	900	-	800	Mbps
	$FMAX_{IDESx}$	1:8/1:10 Gearbox maximum serial input rate	-	1100	-	1000	-	900	Mbps
	$FMAX_{ODDR}$	2:1 Gearbox maximum serial output rate	-	400	-	350	-	300	Mbps
	$FMAX_{OSER4}$	4:1 Gearbox maximum serial output rate	-	800	-	750	-	700	Mbps
	$FMAX_{OSER4}$	7:1 Gearbox maximum serial output rate	-	1000	-	900	-	800	Mbps
	$FMAX_{OSERx}$	8:1/10:1 Gearbox maximum serial output rate	-	1100	-	1000	-	900	Mbps
GW1N-1P5/2	$FMAX_{IDDR}$	1:2 Gearbox maximum serial input rate	-	400	-	350	-	300	Mbps
	$FMAX_{IDES4}$	1:4 Gearbox maximum serial input rate	-	800	-	750	-	700	Mbps
	$FMAX_{IDES7}$	1:7 Gearbox maximum serial input rate	-	1000	-	900	-	800	Mbps

Device	Name	Description	C7/I6		C6/I5		C5/I4		Unit
			Min	Max	Min	Max	Min	Max	
	$FMAX_{IDESx}$	1:8/1:10/1:16 Gearbox maximum serial input rate	-	1200	-	1100	-	1000	Mbps
	$FMAX_{ODDR}$	2:1 Gearbox maximum serial output rate	-	400	-	350	-	300	Mbps
	$FMAX_{OSER4}$	4:1 Gearbox maximum serial output rate	-	800	-	750	-	700	Mbps
	$FMAX_{OSER7}$	7:1 Gearbox maximum serial output rate	-	1000	-	900	-	800	Mbps
	$FMAX_{OSERx}$	8:1/10:1/16:1 Gearbox maximum serial output rate	-	1200	-	1100	-	1000	Mbps

Note!

- The LVDS IO speed can be up to 1Gbps, but note that for the 1:4 Gearbox and 1:2 Gearbox, the internal core may not be able to reach the corresponding speed.
- Drive Strength=3.5 mA.

Table 3-18 Single-ended IO Fmax

Name	Min. Value of Fmax (MHz)	
	Drive Strength = 4mA	Drive Strength > 4mA
LVTTL33	150	300
LVCMOS33	150	300
LVCMOS25	150	300
LVCMOS18	150	300
LVCMOS15	150	200
LVCMOS12	150	150

Note!

Test load = 30pF.

3.4.5 Clock and I/O Switching Characteristics

Table 3-19 External Switching Characteristics

Device	Name	C7/I6	C6/I5	C5/I4	Unit
		Typ.	Typ.	Typ.	
GW1N-1	HCLK Tree delay	1	1.2	1.4	ns
	PCLK Tree delay(GCLK0~5)	2.2	2.4	2.6	ns

Device	Name	C7/I6	C6/I5	C5/I4	Unit
		Typ.	Typ.	Typ.	
	PCLK Tree delay(GCLK6~7)	2.4	2.7	2.9	ns
	Pin-LUT-Pin Delay	4	4.3	4.6	ns
GW1N-1P5	HCLK Tree delay	0.6	0.8	1.1	ns
	PCLK Tree delay(GCLK0~5)	1.8	2.1	2.4	ns
	PCLK Tree delay(GCLK6~7)	2.1	2.5	2.8	ns
	Pin-LUT-Pin Delay	2.5	3	3.5	ns
GW1N-2	HCLK Tree delay	0.6	0.8	1.1	ns
	PCLK Tree delay(GCLK0~5)	1.8	2.1	2.4	ns
	PCLK Tree delay(GCLK6~7)	2.1	2.5	2.8	ns
	Pin-LUT-Pin Delay	2.5	3	3.5	ns
GW1N-4	HCLK Tree delay	-	1	1.2	ns
	PCLK Tree delay(GCLK0~5)	-	2.2	2.5	ns
	PCLK Tree delay(GCLK6~7)	-	2.5	2.8	ns
	Pin-LUT-Pin Delay	-	4.2	4.5	ns
GW1N-9	HCLK Tree delay	0.8	1	1.2	ns
	PCLK Tree delay(GCLK0~5)	2	2.2	2.5	ns
	PCLK Tree delay(GCLK6~7)	2.2	2.5	2.8	ns
	Pin-LUT-Pin Delay	4	4.2	4.5	ns

3.4.6 On-chip Oscillator Switching Characteristics

Table 3-20 On-chip Oscillator Parameters

Name	Description		Min.	Typ.	Max.
f_{MAX}		GW1N-4	97.25MHz	105MHz	112.85MHz

Name	Description		Min.	Typ.	Max.
	On-chip Oscillator Output Frequency (0 ~ +85℃)	GW1N-1	114MHz	120MHz	126MHz
		GW1N-1P5/2/9	118.75MHz	125MHz	131.25MHz
	On-chip Oscillator Output Frequency (-40 ~ +100℃)	GW1N-4	91.85MHz	105MHz	118.25MHz
		GW1N-1	108MHz	120MHz	132MHz
		GW1N-1P5/2/9	112.5MHz	125MHz	137.5MHz
t_{DT}	Output Clock Duty Cycle		43%	50%	57%
t_{OPJIT}	Output Clock Period Jitter		0.01UIPP	0.012UIPP	0.02UIPP

3.4.7 PLL Switching Characteristics

Table 3-21 PLL Timing Parameters

Name	Description	GW1N-1		GW1N-1P5/ GW1N-2		GW1N-4			GW1N-9		Unit
		C6/I5	C5/I4	C7/I6	C6/I5	C7/I6	C6/I5	C5/I4	C7/I6	C6/I5	
F_{INMAX}	Maximum Input Clock Frequency	400	320	400	400	-	400	320	400	400	MHz
F_{INMIN}	Minimum Input Clock Frequency	3	3	3	3	-	3	3	3	3	MHz
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector	400	320	400	400	-	400	320	400	400	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	3	3	3	3	-	3	3	3	3	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max									
F_{INDUTY}	Minimum Allowable Input Duty Cycle: 3-49 MHz	25	25	25	25	-	25	25	25	25	%

Name	Description	GW1N-1		GW1N-1P5/ GW1N-2		GW1N-4			GW1N-9		Unit
		C6/I5	C5/I4	C7/I6	C6/I5	C7/I6	C6/I5	C5/I4	C7/I6	C6/I5	
	Minimum Allowable Input Duty Cycle: 50-199 MHz	30	30	30	30	-	30	30	30	30	%
	Minimum Allowable Input Duty Cycle: 200-399 MHz	35	35	35	35	-	35	35	35	35	%
F_{VCOMIN}	Minimum PLL VCO Frequency	400	320	400	400	-	400	320	400	400	MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	900	720	800	800	-	1000	800	1200	1200	MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the PLL Outputs	+/-50	+/-50	+/-50	+/-50	-	+/-50	+/-50	+/-50	+/-50	ps
$T_{JITTER_CCJ_HCLK}$[3]	PLL Output cycle-cycle Jitter Thru HCLK≥ 100MHz	<300	<300	<300	<300	-	<300	<300	<300	<300	ps
	PLL Output cycle-cycle Jitter Thru HCLK <100MHz	<30	<30	<30	<30	-	<30	<30	<30	<30	mUI
	PLL Output cycle-cycle Jitter Thru PCLK≥ 100MHz	<400	<400	<400	<400	-	<400	<400	<400	<400	ps
	PLL Output cycle-cycle Jitter Thru PCLK<100MHz	<40	<40	<40	<40	-	<40	<40	<40	<40	mUI
T_{JITTER_P}	PLL Output	<300	<300	<300	<300	-	<300	<300	<300	<300	ps

Name	Description	GW1N-1		GW1N-1P5/ GW1N-2		GW1N-4			GW1N-9		Unit
		C6/I5	C5/I4	C7/I6	C6/I5	C7/I6	C6/I5	C5/I4	C7/I6	C6/I5	
J_PCLK	period Jitter Thru HCLK⩾ 100MHz										
	PLL Output period Jitter Thru HCLK <100MHz	<30	<30	<30	<30	-	<30	<30	<30	<30	mUI
	PLL Output period Jitter Thru PCLK ⩾100MHz	<400	<400	<400	<400	-	<400	<400	<400	<400	ps
	PLL Output period Jitter Thru PCLK <100MHz	<40	<40	<40	<40	-	<40	<40	<40	<40	mUI
$T_{OUTDUTY}$ [1],[4]	PLL Output Clock Duty Cycle Precision	<50	<50	<50	<50	-	<50	<50	<50	<50	mUI
$T_{LOCKMAX}$	PLL Maximum Lock Time	1	1	1	1	-	1	1	1	1	ms
F_{OUTMAX}	PLL Maximum Output Frequency	450	360	800	800	-	500	400	600	600	MHz
F_{OUTMIN}[2]	PLL Minimum Output Frequency	3.125	2.5	3.125	3.125	-	3.125	2.5	3.125	3.125	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max									
$R_{STMINPULSE}$	Minimum Reset Pulse Width	10	10	10	10	-	10	10	10	10	ns

Note!

- [1] These test values are based on integer frequency division.
- [2] In cascade mode, multiple dividers can be connected in series to obtain a lower output frequency.

- [3] The output jitter is related to the input source. These test values are based on the case where a low-jitter crystal oscillator is used as the input source.
- [4] The duty cycle on the IO is also affected by the clock tree.

3.5 User Flash Characteristics

3.5.1 DC Characteristics

(T_J = -40~+100℃, V_{CC} = 0.95~1.05V, V_{CCX} = 1.7~3.45V, V_{SS} = 0V)

Table 3-22 GW1N-1 User Flash DC Characteristics

Symbol	Description	Specification			Unit
		Min.	Typ.	Max.	
Tj	Junction Temperature	-40	25	100	℃
Ilkg	Leakage current	–	–	1[1]	μA
Isb	Standby current	–	–	3（Ta=25）	μA
		–	–	20（Ta=85）	
Icc0	Idle current	–	–	1.3	mA
Icc1	Read current	–	–	2（Rmod=00）	mA
		–	–	2.5（Rmod=01）	mA
		–	–	3（Rmod=1x）	mA
Icc2	Page write current	–	–	2	mA
Icc3	Program/erase current	–	–	3	mA

Note!

[1] The leakage current of the Flash is included in the leakage current of the device, see Table 3-4 Hot Socketing Specifications.

Table 3-23 GW1N-2/4/9 User Flash DC Characteristics(I)

Symbol	Description	Specification			Unit
		Min.	Typ.	Max.	
Tj	Junction Temperature	-40	25	125	℃

Table 3-24 GW1N-2/4/9 User Flash DC Characteristics(II)[1], [4]

Name	Parameter	Max.		Unit	Wake-up time	Condition
		V_{CC}[3]	V_{CCX}			
Read mode(w/I 25ns)	I_{CC1}[2]	2.19	0.5	mA	NA	Minimum clock period, 100% duty cycle , VIN = “1/0”
Write mode		0.1	12	mA	NA	–
Erase mode		0.1	12	mA	NA	–

Name	Parameter	Max.		Unit	Wake-up time	Condition
		V_{CC}[3]	V_{CCX}			
Page erase mode		0.1	12	mA	NA	–
Static read current (25-50ns)	I_{CC2}	980	25	μA	NA	XE=YE=SE="1", between T=T_{acc} and T=50ns, the I/O current is 0mA. After T=50ns, the internal timer turns off read mode, and the I/O current turns out to be the standby current.
Standby mode	I_{SB}	5.2	20	μA	0	V_{SS}, V_{CCX}, and V_{CC}

Note!

- [1] These values are average DC currents and the peak currents will be higher than these average currents.
- [2] I_{CC1} calculation in different cycle time of T_{new}.
  - $T_{new} < T_{acc}$: not allowed.
  - $T_{new} = T_{acc}$: see the table above.
  - $T_{acc} < T_{new} - 50ns$: $I_{CC1}(new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + I_{CC2}$
  - $T_{new} > 50ns$: $I_{CC1}(new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + 50ns*I_{CC2}/T_{new} + I_{SB}$
  - $t > 50ns$: $I_{CC2} = I_{SB}$
- [3] V_{CC} must be greater than 1.08V from time zero of the wake-up time.
- [4] The leakage current of the Flash is included in the leakage current of the device, see Table 3-4 Hot Socketing Specifications.

3.5.2 Timing Parameters

(T_J = -40~+100℃, V_{CC} = 0.95~1.05V, V_{CCX} = 1.7~3.45V, V_{SS} = 0V)

Table 3-25 GW1N-1 User Flash Parameters

Symbol	Description	Specification			Unit
		Min.	Typ.	Max.	
Taa	Data access time	–	–	38	ns
Tcy	Read cycle time	43	–	–	ns
Taw	Aclk clock pulse high time	10	–	–	ns
Tawl	Aclk clock pulse low time	10	–	–	ns
Tas	Setup time	3	–	–	ns
Tah	Hold time	3	–	–	ns
Toz	Oe low to Dout Hi-Z	–	–	2	ns
Toe	Oe high to Dout valid	–	–	2	ns
Twcy	Write cycle time	40	–	–	ns
Tpw	Pw clock pulse high time	16	–	–	ns
Tpwl	Pw clock pulse low time	16	–	–	ns
Tpas	Page address setup time	3	–	–	ns
Tpah	Page address hold time	3	–	–	ns
Tds	Data setup time	16	–	–	ns
Tdh	Data hold time	3	–	–	ns
Ts0	Sequence 0 cycle time	6	–	–	μs
Ts1	Sequence 1 cycle time	15	–	–	μs
Ts2p	Aclk to Pe rise setup time	5	–	10	μs
Ts3	Sequence 3 cycle time	5	–	10	μs
Tps3	Pe fall to Aclk setup time	60	–		μs
Tpe	Erase time at Mode=1000	5.7	6	6.3	ms
	Program time at Mode=1100	1.9	2	2.1	ms
	Pre-program time at Mode=11xx	190	200	210	us

Table 3-26 GW1N-1P5/2/4/9 User Flash Parameters[1], [4], [5]

User Mode	Parameter	Symbol	Min.	Max.	Unit
Access time	WC1	T_{acc}[2]	-	25	ns
	TC		-	22	ns
	BC		-	21	ns
	LT		-	21	ns
	WC		-	25	ns
Program/Erase to data storage setup time		T_{nvs}	5	-	μs
Data storage hold time		T_{nvh}	5	-	μs

User Mode	Parameter	Symbol	Min.	Max.	Unit
Data storage hold time(mass erase)		T_{nvh1}	100	-	μs
Data storage to program setup time		T_{pgs}	10	-	μs
Program hold time		T_{pgh}	20	-	ns
Program time		T_{prog}	8	16	μs
Write prepare time		T_{wpr}	>0	-	ns
Write hold time		T_{whd}	>0	-	ns
Control to program/erase setup time		T_{cps}	-10	-	ns
SE to read control setup time		T_{as}	0.1	-	ns
Positive pulse width of SE		T_{pws}	5	-	ns
Address/data setup time		T_{ads}	20	-	ns
Address/data hold time		T_{adh}	20	-	ns
Data hold time		T_{dh}	0.5	-	ns
Address hold time in read mode	WC1	T_{ah}	25	-	ns
	TC	-	22	-	ns
	BC	-	21	-	ns
	LT	-	21	-	ns
	WC	-	25	-	ns
Negative pulse width of SE		T_{nws}	2	-	ns
Recovery time		T_{rcv}	10	-	μs
Data storage time		T_{hv}[3]	-	6	ms
Erase time		T_{erase}	100	120	ms
Mass erase time		T_{me}	100	120	ms
Wake-up time of power-down to standby		T_{wk_pd}	7	-	μs
Standby hold time		T_{sbh}	100	-	ns
V_{CC} setup time		T_{ps}	0	-	ns
V_{CCX} hold time		T_{ph}	0	-	ns

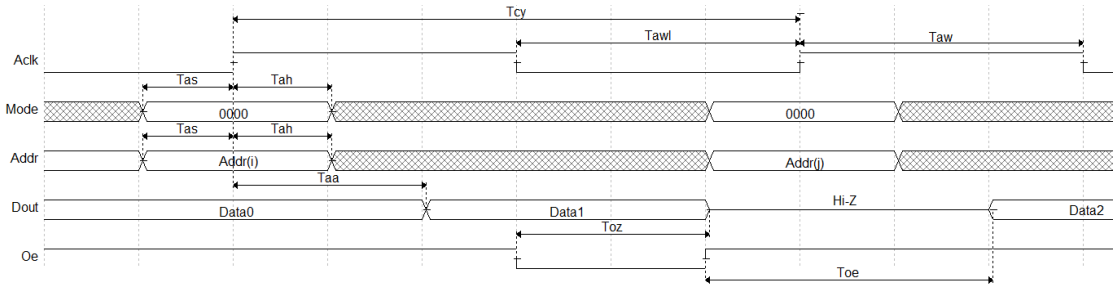
Note!

- [1] The values are simulation data and are subject to change.

- [2]After XADR, YADR, XE, and YE are valid, T_{acc} starts at the rising edge of SE. DOUT will be kept before the next valid read operation starts.
- [3] T_{hv} is the cumulative high voltage programming time to the same row before next erase. The same address cannot be programmed (either “0” or “1”) more than 2 times before the next erase and the same bit-cell can't be programmed(“0”) more than 2 times before the next erase. The program behavior is limited based on above constraints of whichever is satisfied first.
- [4] All waveforms have a 1ns rising time and a 1ns falling time.
- [5] Control signals(X, YADR, XE, and YE) need to be held for at least T_{acc}, which starts at the rising edge of SE.

3.5.3 Timing Diagrams (GW1N-1)

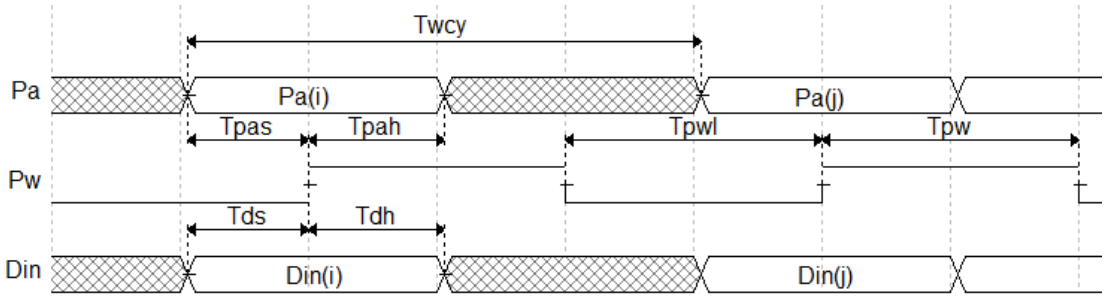
Figure 3-1 Read Mode



Note!

Read cycles when Seq=0. The Addr signal contains Ra, Ca, Rmod, and Rbytesel.

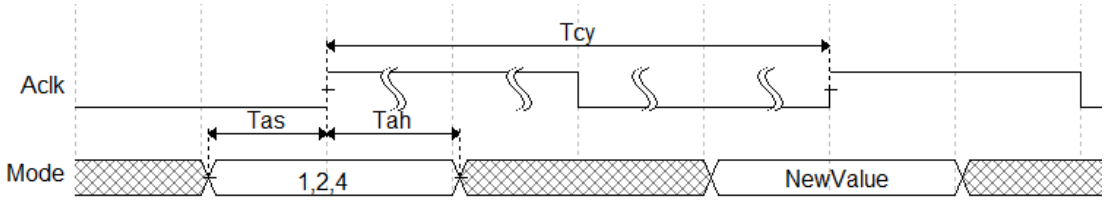
Figure 3-2 Write Page Latch Mode



Note!

Write page latch cycles when Seq=0, Mode=0000.

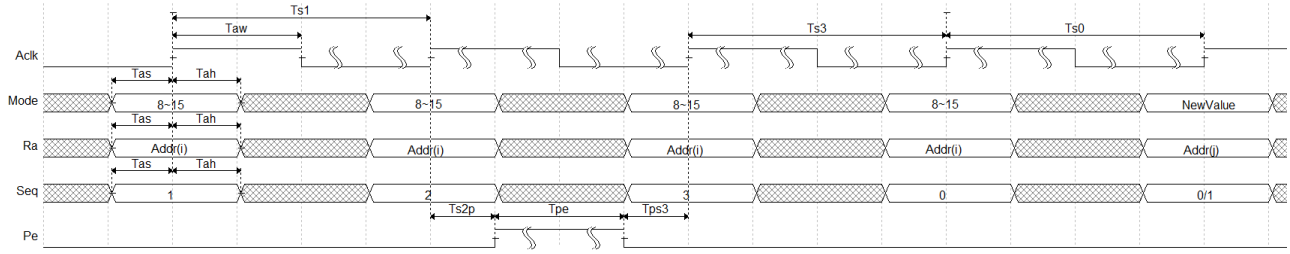
Figure 3-3 Clear Page Latch Mode



Note!

The timing parameters of setting PEP and writing data to all pages are the same as those of clearing page latches, except that the MODE value is different.

Figure 3-4 High Level Cycles



3.5.4 Timing Diagrams (GW1N-1P5/2/4/9)

Figure 3-5 Read Timing

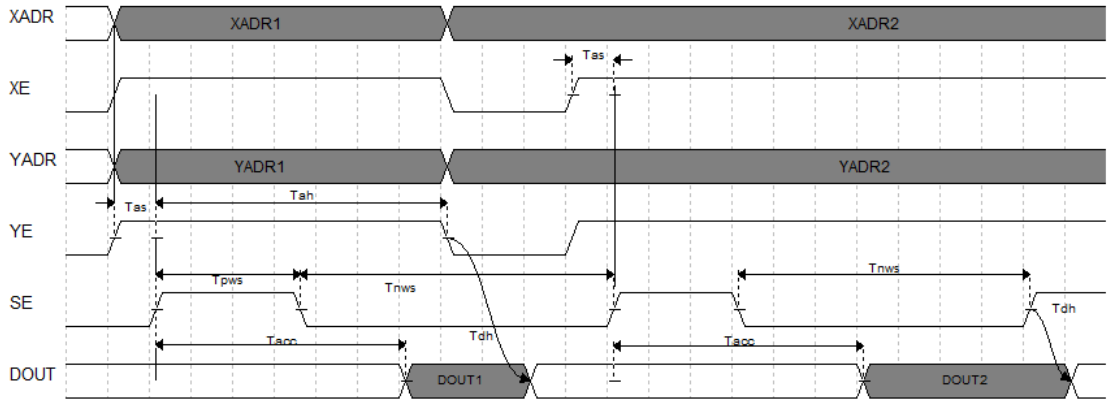


Figure 3-6 Program Timing

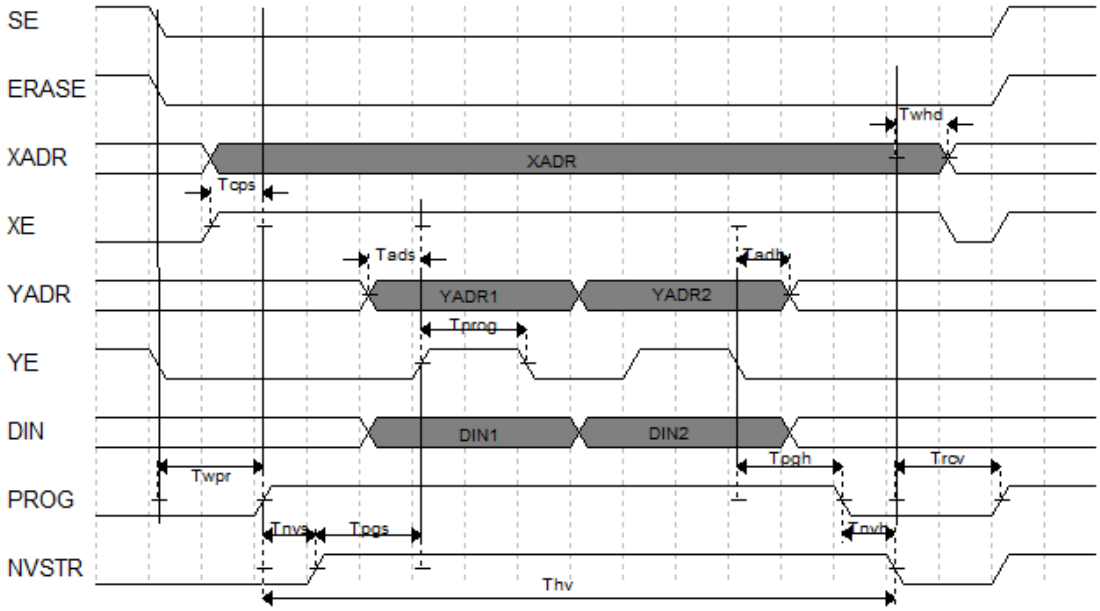
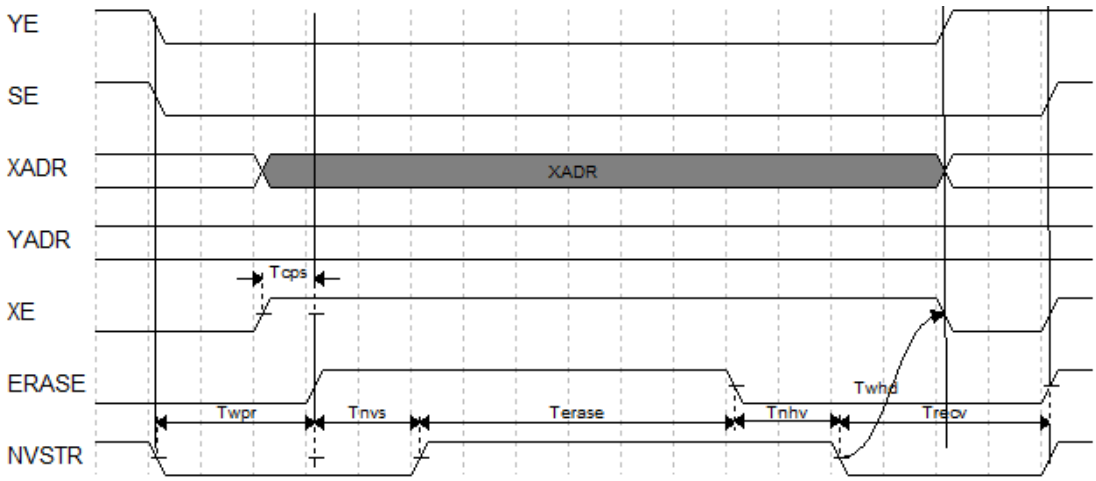


Figure 3-7 Erase Timing



3.6 Configuration Interface Timing Specification

The GW1N series of FPGA products support seven GowinCONFIG modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, CPU, and I^2C Slave. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

4 Ordering Information

4.1 Part Naming

Note!

- For more information about the packages, please refer to 1.2 Product Resources and 1.3 Package Information.

Figure 4-1 Part Naming Examples – ES

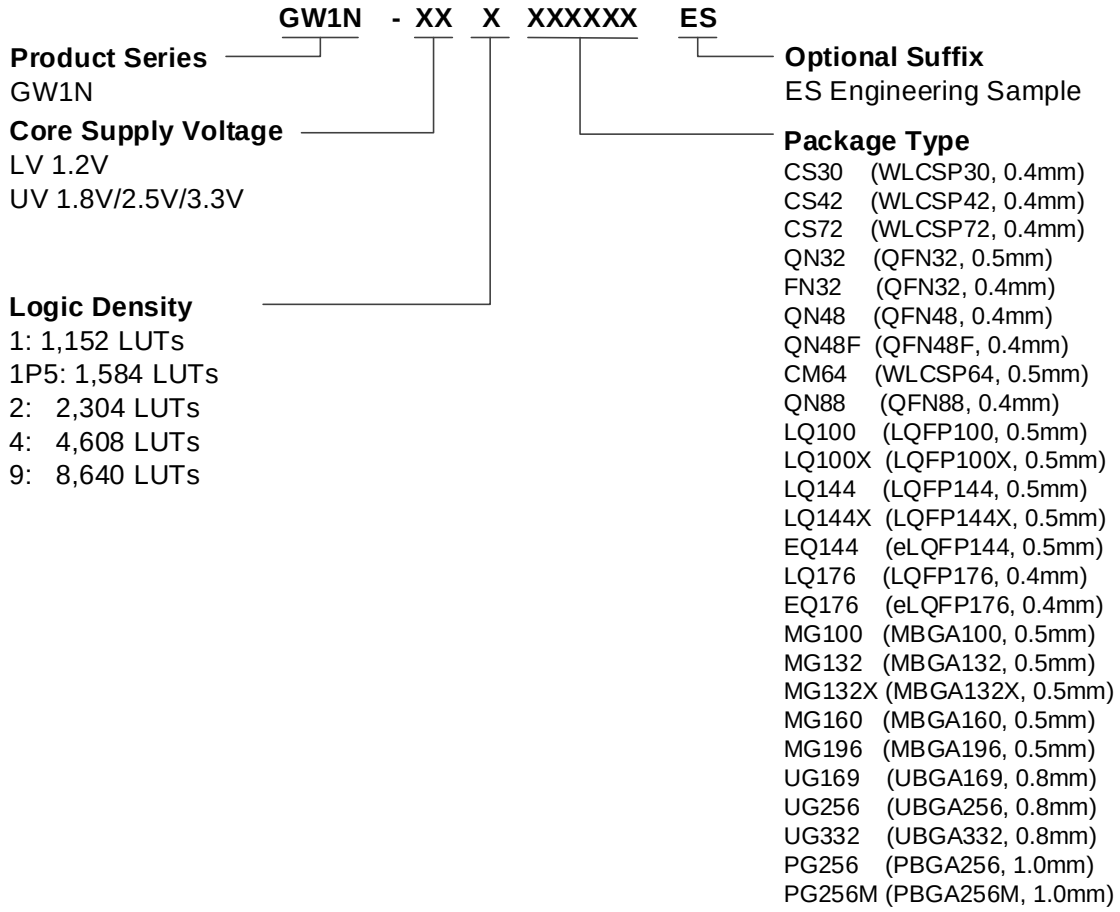
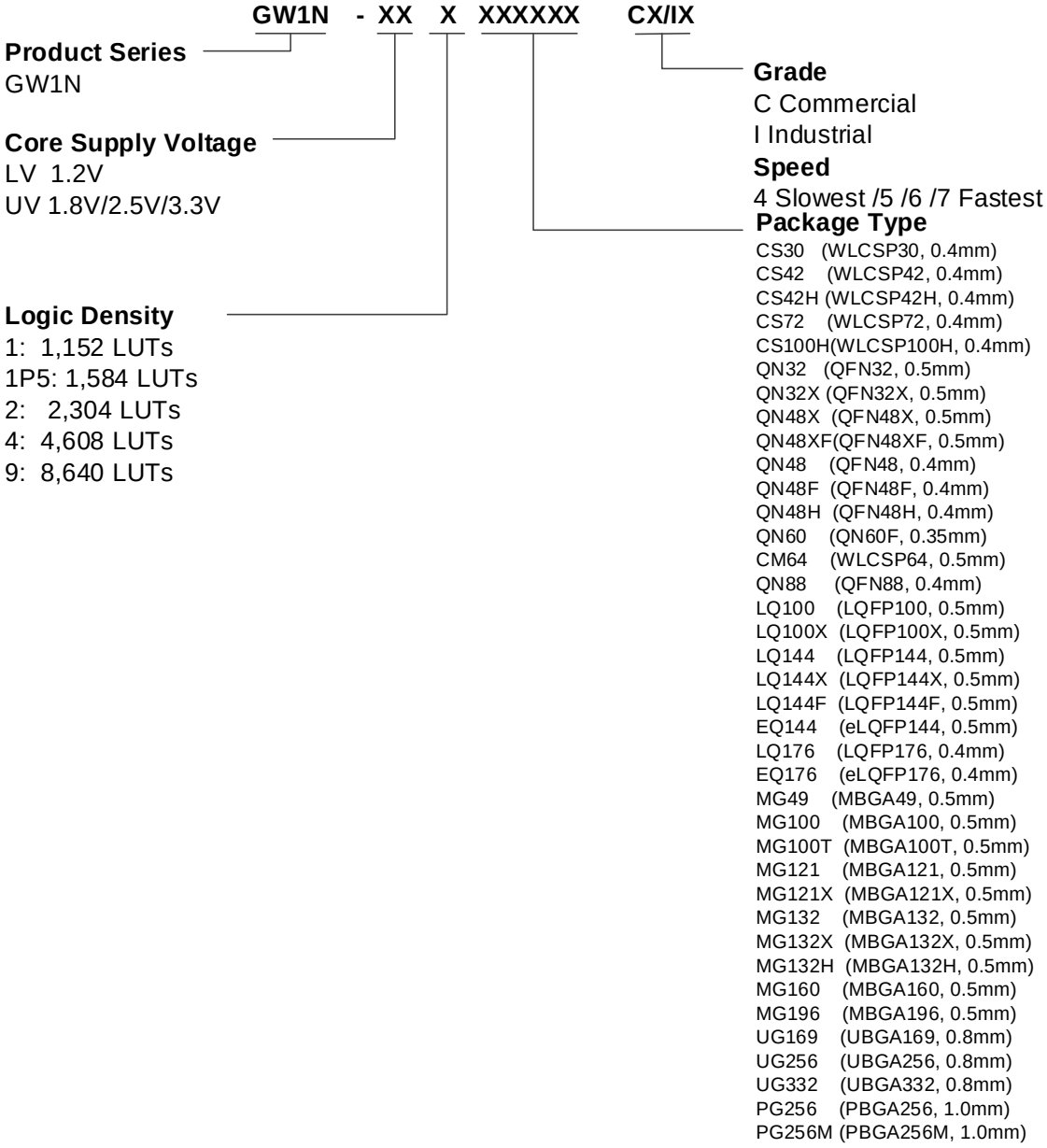


Figure 4-2 Part Naming Examples – Production



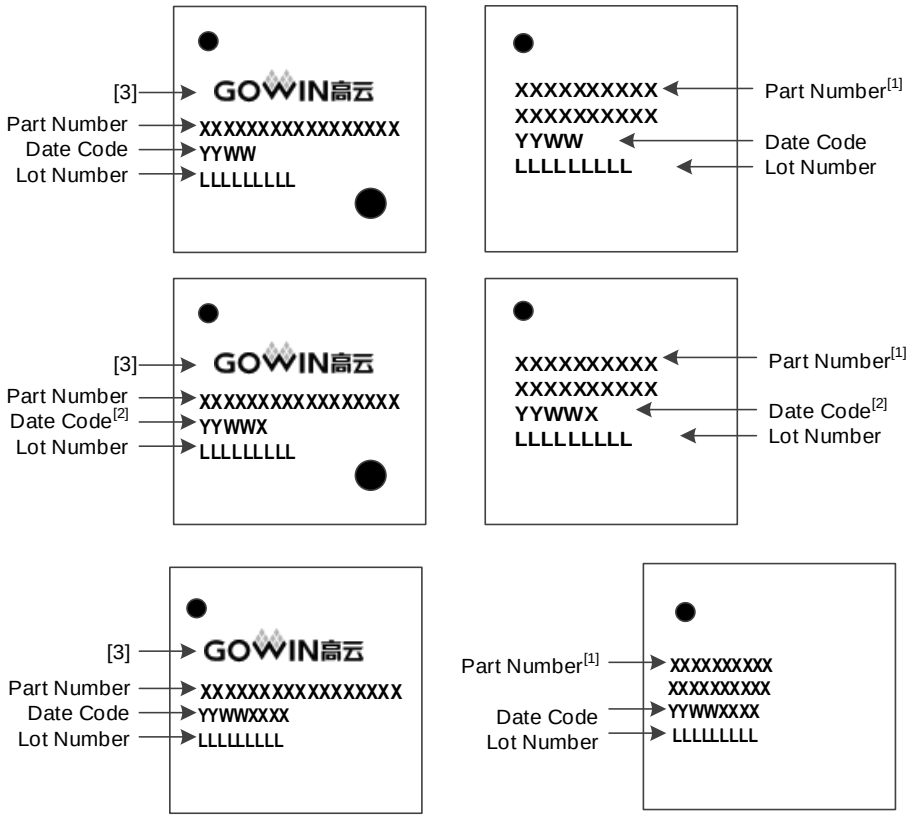
Note!

- The LittleBee family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in Gowin’s part name marking for one device. GOWIN devices are screened using industrial standards, so the same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the chip meets speed grade 7 in commercial grade applications, its speed grade will be 6 in industrial grade applications.

4.2 Package Markings

Gowin's devices have markings on the their surfaces, as shown in Figure 4-3 and Figure 4-4.

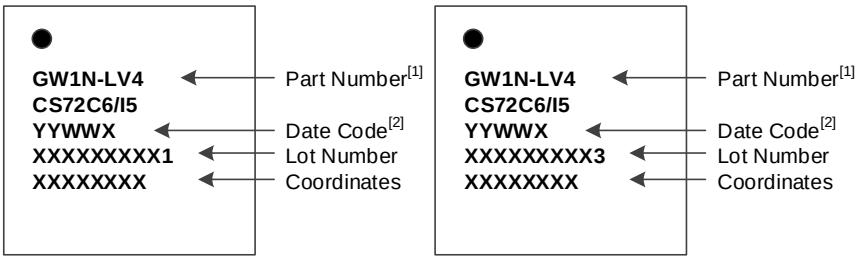
Figure 4-3 Package Marking Examples



Note!

- [1] The first two lines in the right figure(s) above are both the "Part Number".
- [2] The fifth character of the Date Code denotes the version of the device.
- [3] Whether the package marking bears the Gowin Logo or not depends on the package type, package size, and Part Number length. The above figure are only examples of the package markings.

Figure 4-4 Package Marking Examples(GW1N-LV4CS72C6/I5)



Note!

- [1] The first two lines in the right figure(s) above are both the "Part Number".

- [2] The fifth character of the Date Code denotes the version of the device.

5 About This Guide

5.1 Purpose

This datasheet provides a comprehensive overview of the GW1N series of FPGA products, including their features, resources, architecture, AC/DC characteristics, and ordering details.

5.2 Related Documents

The latest documents are available at www.gowinsemi.com.

- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG103, GW1N series of FPGA Products Package and Pinout Manual
- UG107, GW1N-1 Pinout
- UG105, GW1N-4 Pinout
- UG114, GW1N-9 Pinout
- UG171, GW1N-2 Pinout
- UG174, GW1N-1P5 Pinout

5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are shown in Table 5-1.

Table 5-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Section

Terminology and Abbreviations	Full Name
CLU	Configurable Logic Unit
CRU	Configurable Routing Unit
CS	WLCSP
CSI	Camera Serial Interface
DCS	Dynamic Clock Selector
DP	True Dual Port 16K BSRAM
DQCE	Dynamic Quadrant Clock Enable
DSI	Display Serial Interface
DSP	Digital Signal Processing
FF	Flip-Flop
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable I/O
IOB	Input/Output Block
LQ	LQFP
LUT4	4-input Look-up Table
MG	MBGA
MIPI	Mobile Industry Processor Interface
PG	PBGA
PLL	Phase-locked Loop
QN	QFN
REG	Register
SDP	Semi-Dual Port 16K BSRAM
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
TBD	To Be Determined
UG	UBGA

5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail：support@gowinsemi.com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