Version History

Date	Version	Description
10/24/2019	1.0E	Initial version published. QN48 and QN48E packages supported.
12/05/2019	1.1E	Pin definitions improved.
09/11/2020	1.2E	The descriptions of pin BLE added. Pin p in Pin List removed.
12/14/2021	1.3E	Pin definitions updated. The notes of JTAG configuration pin optimized.
10/20/2022	1.3.1E	Pin definitions updated. The notes of JTAG configuration pin optimized.
05/04/2023	1.3.2E	The notes of QN48/QN48E in Power sheet added. The description of CLKHOLD_N pin in Pin Definitions sheet updated.
06/30/2023	1.3.3E	The descriptions of pin definitions and info. for MODE0, MODE1, MODE2 pins optimized.
11/15/2024	1.3.4E	The description of EPAD pin in Pin Definitions sheet added. The I/O descriptions of Ready and Done pins in Pin Definitions sheet optimized.

Pin Name	I/O	Description
User I/O		
IO[End][Row/Column Number][A/B]	I/O	[End] indicates the pin location, including L(left), R(right), B(bottom), and T(top).
		[Row/Column Number] indicates the pin row/column number. If [End] is T(top) or B(bottom), the pin indicates the column number of the corresponding CFU. If [End] is L(left) or R(right), the pin indicates the row number of the corresponding CFU.
		[A/B] indicates differential signal pair information.
Multi-Function Pins		
IO[End][Row/Column Number][A/B]/MMM		/MMM represents one or more of the other functions in addition to being general purpose user I/O. When these functions are not in use, these pins can be used as user I/O.
D0	I/O	Data port D0 in CPU mode
D1	I/O	Data port D1 in CPU mode
D2	I/O	Data port D2 in CPU mode
D3	I/O	Data port D3 in CPU mode
D4	I/O	Data port D4 in CPU mode
D5	I/O	Data port D5 in CPU mode
D6	I/O	Data port D6 in CPU mode
D7	I/O	Data port D7 in CPU mode
WE_N	I	Select data input/output of D[7:0] in CPU mode.0: Write;1: Read.
DOUT	O	Data output in SERIAL mode
DIN	I, internal weak pull-up	Data input in SERIAL mode
TMS	I, internal weak pull-up	Serial mode input in JTAG mode
TCK	I	Serial clock input in JTAG mode
TDO	O	Serial data output in JTAG mode
TDI	I, internal weak pull-up	Serial data input in JTAG mode
JTAGSEL_N	I, internal weak pull-up	Reconfigure JTAG download function signal
RECONFIG_N	I, internal weak pull-up	Global reset GowinCONFIG logic signal, active low
FASTRD_N	I	Access SPI FLASH to select signal. Low, Fast Read mode; High, Read mode.
DONE[1]	O, internal weak pull-up	High, the programming configuration has been completed successfully; Low, the programming configuration has not been completed or failed.
	I, internal weak pull-up	When the DONE signal is low, delay the chip to activate. Activate the chip until the DONE signal is high.
READY[1]	I/O, internal weak pull-up	High, the device can be programmed and configured currently; Low, the device cannot be programmed and configured currently.
MI	I	MI in MSPI mode

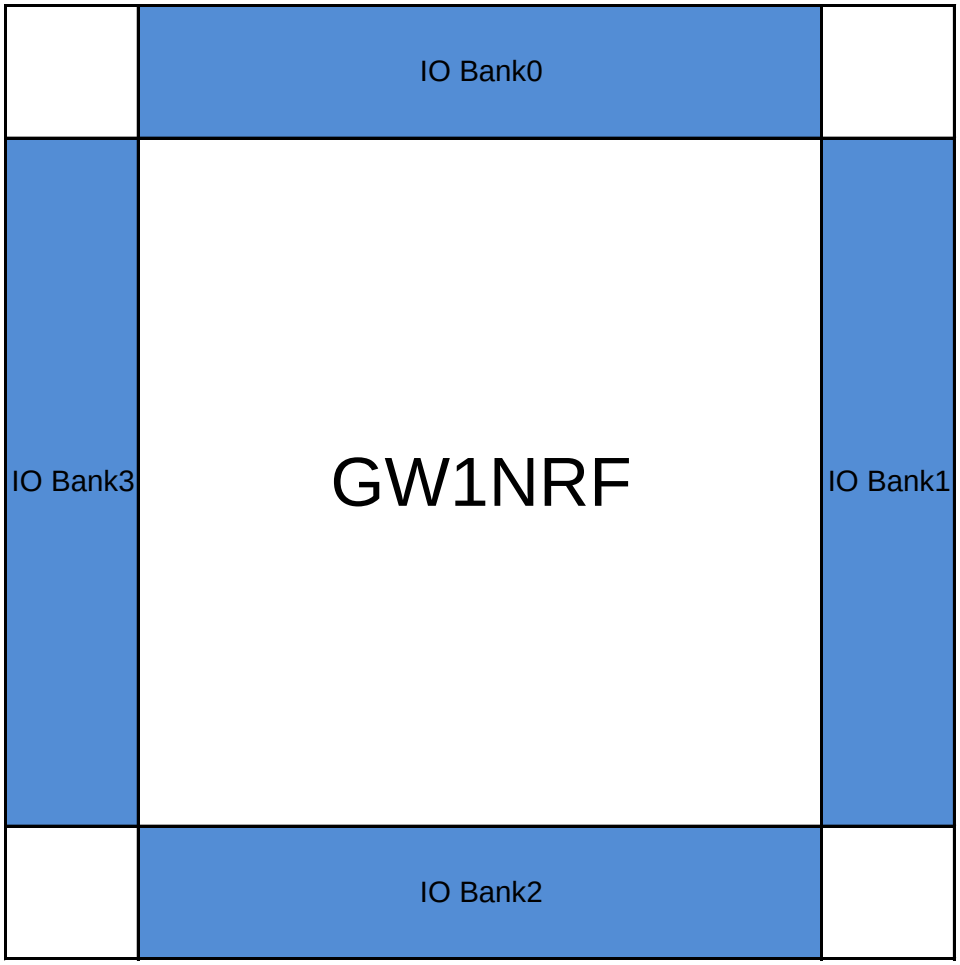
Pin Name	I/O	Description
MO	O	MO in MSPI mode
MCS_N	O	Enable signal MCS_N in MSPI mode, active-low
MCLK	O	Clock output MCLK in MSPI mode, with default frequency of 2.5Mhz
SCLK	I	Clock input in SSPI, SERIAL, and CPU modes
SO	O	SO in SSPI mode
SI	I/O	SI in SSPI mode
SSPI_CS_N	I/O	Enable signal SSPI_CS_N in SSPI mode, active-low, and internal weak pull-up
CLKHOLD_N	I, internal weak pull-up	Active-high in SSPI mode; Active-low in CPU mode.
GCLKC_[x]	I	Differential input pin of GCLKT_[x], C(Comp), [x] is global clock number[2]
GCLKT_[x]	I	Global clock input pin, T(True), [x] is global clock number
LPLL_C_fb/RPLL_C_fb	I	Left/Right PLL feedback input pin, C(Comp)
LPLL_T_fb/RPLL_T_fb	I	Left/Right PLL feedback input pin, T(True)
LPLL_C_in/RPLL_C_in	I	Left/Right PLL clock input pin, C(Comp)
LPLL_T_in/RPLL_T_in	I	Left/Right PLL clock input pin, T(True)
MODE2	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE1	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
MODE0	I, internal weak pull-up	GowinCONFIG modes selection pin; if this pin is marked as “VCCIO”, it's internally powered; if this pin is marked as "GND", it's internally grounded.
BLE		
GPIO [Number]	I/O	BLE logic input and output pin
ANT	I/O	RF single-ended antenna
ENABLE	I	The chip is enabled. When the enable pin is low, the chip does not work.
LF_XIN	I	32.768kHz XTAL
LF_XOUT	O	32.768kHz XTAL
XIN	I	48MHz XTAL
XOUT	O	48MHz XTAL
VCCGPIO	Power	GPIO voltage level of internal MCU
MCUVCC	Power	MCUVCC, generated by DCDC switch, external inductor, and capacitor.
SW_DCDC	Power	Power switch pin connects this pin to the switch node of the inductor, plus 4.7uH inductance, 2.2uF/4.7uF capacitance.

Pin Name	I/O	Description
VBAT1	Power	DCDC power supply voltage
VBAT2	Power	Power supply voltage
Other Pins		
NC	NA	Reserved
VSS	NA	Ground
VCC	NA	Power supply pin of core voltage
VCCIO#	NA	Power supply pin of I/O voltage for I/O BANK#
VCCX	NA	Power supply pin of auxiliary voltage
EPAD	NA	Exposed pad. Connect to ground.

Note!

[1] The default state of READY/DONE is open-drain output, internal weak pull-up. DONE outputs 0 during configuration.

[2] When the input is single-ended, GCLKC_[x] pin is not a global clock.



Note!

[1] Each Bank has independent reference voltage (VREF).

[2] You can select to use IOB internal VREF (equals to 0.5 * VCCIO).

[3] You can also select to use external VREF input (use any IO pins as external VREF input).

Note!
VCCX should be greater than or equal to VCCIO.

Recommended Operating Conditions of QN48 Package in GW1NRF-4B				
Name	**Description**		**Min.**	**Max.**
VCC	Core voltage	LV: Core voltage	1.14V	1.26V
		UV: Core voltage	1.71V	3.6V
VCCIO0/VCCIO3	I/O Bank power supply voltage, VCCIO0 and VCCIO3 are internally short-circuited.		1.14V	3.6V
VCCIO1/VCCIO2	I/O Bank power supply voltage, VCCIO1 and VCCIO2 are internally short-circuited.		1.14V	3.6V
VCCX	Auxiliary voltage		2.375V	3.6V

Note !
It is highly recommended that the EPAD connect to GND, but not a requirement.

Recommended Operating Conditions of QN48E Package in GW1NRF-4B			
Name	**Description**	**Min.**	**Max.**
VCC	Core voltage	1.14V	1.26V
VCCIO0/VCCIO3	I/O Bank power supply voltage, VCCIO0 and VCCIO3 are internally short-circuited.	1.14V	3.6V
VCCIO1/VCCIO2	I/O Bank power supply voltage, VCCIO1 and VCCIO2 are internally short-circuited.	1.14V	3.6V
VCCX	Auxiliary voltage	2.375V	3.6V

Note !
It is highly recommended that the EPAD connect to GND, but not a requirement.

Note!

[1][2] In package QN48 and QN48E, IOL10B/TCK and GPIO8/TCK share pin 5 and IOL10A/TMS and GPIO11/TMS share pin 7.

[3][4] The configuration pin TDO of GW1NRF-4B is connected to the configuration pin TDI of BLE, forming a JTAG daisy chain.

[5] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
IOB10A	I/O	2		True_of_IOB10B	NONE		
IOB10B	I/O	2		Comp_of_IOB10A	NONE		
IOB11A	I/O	2		True_of_IOB11B	NONE		
IOB11B	I/O	2		Comp_of_IOB11A	NONE		
IOB12A	I/O	2		True_of_IOB12B	TRUE		
IOB12B	I/O	2		Comp_of_IOB12A	TRUE		
IOB13A	I/O	2		True_of_IOB13B	NONE		
IOB13B	I/O	2		Comp_of_IOB13A	NONE		
IOB14A	I/O	2		True_of_IOB14B	TRUE		
IOB14B	I/O	2		Comp_of_IOB14A	TRUE		
IOB15A	I/O	2		True_of_IOB15B	NONE		
IOB15B	I/O	2		Comp_of_IOB15A	NONE		
IOB16A	I/O	2		True_of_IOB16B	TRUE		
IOB16B	I/O	2		Comp_of_IOB16A	TRUE		
IOB17A	I/O	2		True_of_IOB17B	NONE		
IOB17B	I/O	2		Comp_of_IOB17A	NONE		
IOB18A	I/O	2		True_of_IOB18B	TRUE		
IOB18B	I/O	2		Comp_of_IOB18A	TRUE		
IOB19A/GCLKT_5	I/O	2	GCLKT_5	True_of_IOB19B	NONE	17	17
IOB19B/GCLKC_5	I/O	2	GCLKC_5	Comp_of_IOB19A	NONE	18	18
IOB20A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB20B	TRUE	19	19
IOB20B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB20A	TRUE	20	20
IOB21A	I/O	2		True_of_IOB21B	NONE		
IOB21B	I/O	2		Comp_of_IOB21A	NONE		
IOB22A	I/O	2		True_of_IOB22B	TRUE		
IOB22B	I/O	2		Comp_of_IOB22A	TRUE		
IOB23A	I/O	2		True_of_IOB23B	NONE		
IOB23B	I/O	2		Comp_of_IOB23A	NONE		
IOB24A	I/O	2		True_of_IOB24B	TRUE		
IOB24B	I/O	2		Comp_of_IOB24A	TRUE		

Note!

[1][2] In package QN48 and QN48E, IOL10B/TCK and GPIO8/TCK share pin 5 and IOL10A/TMS and GPIO11/TMS share pin 7.

[3][4] The configuration pin TDO of GW1NRF-4B is connected to the configuration pin TDI of BLE, forming a JTAG daisy chain.

[5] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
IOB25A	I/O	2		True_of_IOB25B	NONE		
IOB25B	I/O	2		Comp_of_IOB25A	NONE		
IOB26A	I/O	2		True_of_IOB26B	TRUE	21	21
IOB26B	I/O	2		Comp_of_IOB26A	TRUE	22	22
IOB27A	I/O	2		True_of_IOB27B	NONE		
IOB27B	I/O	2		Comp_of_IOB27A	NONE		
IOB28A	I/O	2		True_of_IOB28B	NONE		
IOB28B	I/O	2		Comp_of_IOB28A	NONE		
IOB29A	I/O	2		True_of_IOB29B	NONE		
IOB29B	I/O	2		Comp_of_IOB29A	NONE		
IOB2A	I/O	2		True_of_IOB2B	TRUE		
IOB2B	I/O	2		Comp_of_IOB2A	TRUE		
IOB30A	I/O	2		True_of_IOB30B	TRUE		
IOB30B	I/O	2		Comp_of_IOB30A	TRUE		
IOB31A	I/O	2		True_of_IOB31B	NONE		
IOB31B	I/O	2		Comp_of_IOB31A	NONE		
IOB32A	I/O	2		True_of_IOB32B	TRUE	23	23
IOB32B	I/O	2		Comp_of_IOB32A	TRUE	24	24
IOB33A	I/O	2		True_of_IOB33B	NONE		
IOB33B	I/O	2		Comp_of_IOB33A	NONE		
IOB34A	I/O	2		True_of_IOB34B	TRUE		
IOB34B	I/O	2		Comp_of_IOB34A	TRUE		
IOB35A	I/O	2		True_of_IOB35B	NONE		
IOB35B	I/O	2		Comp_of_IOB35A	NONE		
IOB36A	I/O	2		True_of_IOB36B	TRUE		
IOB36B	I/O	2		Comp_of_IOB36A	TRUE		
IOB37A	I/O	2		True_of_IOB37B	NONE		
IOB37B	I/O	2		Comp_of_IOB37A	NONE		
IOB3A	I/O	2		True_of_IOB3B	NONE		

Note!

[1][2] In package QN48 and QN48E, IOL10B/TCK and GPIO8/TCK share pin 5 and IOL10A/TMS and GPIO11/TMS share pin 7.

[3][4] The configuration pin TDO of GW1NRF-4B is connected to the configuration pin TDI of BLE, forming a JTAG daisy chain.

[5] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
IOB3B	I/O	2		Comp_of_IOB3A	NONE		
IOB4A	I/O	2		True_of_IOB4B	TRUE		
IOB4B	I/O	2		Comp_of_IOB4A	TRUE		
IOB5A	I/O	2		True_of_IOB5B	NONE		
IOB5B	I/O	2		Comp_of_IOB5A	NONE		
IOB6A	I/O	2		True_of_IOB6B	TRUE		
IOB6B	I/O	2		Comp_of_IOB6A	TRUE		
IOB7A	I/O	2		True_of_IOB7B	NONE		
IOB7B	I/O	2		Comp_of_IOB7A	NONE		
IOB8A	I/O	2		True_of_IOB8B	TRUE		
IOB8B	I/O	2		Comp_of_IOB8A	TRUE		
IOB9A	I/O	2		True_of_IOB9B	NONE		
IOB9B	I/O	2		Comp_of_IOB9A	NONE		
IOL10A/TMS[1]	I/O	3	TMS	True_of_IOL10B	NONE	7	7
IOL10B/TCK[2]	I/O	3	TCK	Comp_of_IOL10A	NONE	5	5
IOL10C/SCLK	I/O	3	SCLK	True_of_IOL10D	NONE		
IOL10D/TDI	I/O	3	TDI	Comp_of_IOL10C	NONE	6	6
IOL10E/TDO[3]	I/O	3	TDO	True_of_IOL10F	NONE		8
IOL10F/RECONFIG_N	I/O	3	RECONFIG_N	Comp_of_IOL10E	NONE		
IOL10G/DONE	I/O	3	DONE	True_of_IOL10H	NONE		
IOL10H/READY	I/O	3	READY	Comp_of_IOL10G	NONE		
IOL10I	I/O	3		True_of_IOL10J	NONE		
IOL10J	I/O	3		Comp_of_IOL10I	NONE		
IOL11A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL11B	TRUE	8	
IOL11B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL11A	TRUE		
IOL12A	I/O	3		True_of_IOL12B	NONE		
IOL12B	I/O	3		Comp_of_IOL12A	NONE		
IOL13A	I/O	3		True_of_IOL13B	TRUE		

Note!

[1][2] In package QN48 and QN48E, IOL10B/TCK and GPIO8/TCK share pin 5 and IOL10A/TMS and GPIO11/TMS share pin 7.

[3][4] The configuration pin TDO of GW1NRF-4B is connected to the configuration pin TDI of BLE, forming a JTAG daisy chain.

[5] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
IOL13B	I/O	3		Comp_of_IOL13A	TRUE		
IOL14A	I/O	3		True_of_IOL14B	NONE		
IOL14B	I/O	3		Comp_of_IOL14A	NONE		
IOL15A	I/O	3		True_of_IOL15B	TRUE		
IOL15B	I/O	3		Comp_of_IOL15A	TRUE		
IOL16A	I/O	3		True_of_IOL16B	NONE		
IOL16B	I/O	3		Comp_of_IOL16A	NONE		
IOL17A	I/O	3		True_of_IOL17B	TRUE		
IOL17B	I/O	3		Comp_of_IOL17A	TRUE		
IOL18A	I/O	3		True_of_IOL18B	NONE		
IOL18B	I/O	3		Comp_of_IOL18A	NONE		
IOL2A	I/O	3		True_of_IOL2B	TRUE		
IOL2B	I/O	3		Comp_of_IOL2A	TRUE		
IOL3A/JTAGSEL_N/LPLL_T_in	I/O	3	JTAGSEL_N/LPLL_T_in	True_of_IOL3B	NONE	3	3
IOL3B/LPLL_C_in	I/O	3	LPLL_C_in	Comp_of_IOL3A	NONE		
IOL4A/LPLL_T_fb	I/O	3	LPLL_T_fb	True_of_IOL4B	TRUE		
IOL4B/LPLL_C_fb	I/O	3	LPLL_C_fb	Comp_of_IOL4A	TRUE		
IOL5A	I/O	3		True_of_IOL5B	NONE		
IOL5B	I/O	3		Comp_of_IOL5A	NONE		
IOL6A	I/O	3		True_of_IOL6B	TRUE		
IOL6B	I/O	3		Comp_of_IOL6A	TRUE		
IOL7A	I/O	3		True_of_IOL7B	NONE		
IOL7B	I/O	3		Comp_of_IOL7A	NONE		
IOL8A	I/O	3		True_of_IOL8B	TRUE		
IOL8B	I/O	3		Comp_of_IOL8A	TRUE		
IOL9A/GCLKT_7	I/O	3	GCLKT_7	True_of_IOL9B	NONE		
IOL9B/GCLKC_7	I/O	3	GCLKC_7	Comp_of_IOL9A	NONE		
IOR10A/MI/D7	I/O	1	MI/D7	True_of_IOR10B	NONE		
IOR10B/MO/D6	I/O	1	MO/D6	Comp_of_IOR10A	NONE		

Note!

[1][2] In package QN48 and QN48E, IOL10B/TCK and GPIO8/TCK share pin 5 and IOL10A/TMS and GPIO11/TMS share pin 7.

[3][4] The configuration pin TDO of GW1NRF-4B is connected to the configuration pin TDI of BLE, forming a JTAG daisy chain.

[5] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
IOR10C/MCS_N/D5	I/O	1	MCS_N/D5	True_of_IOR10D	NONE		
IOR10D/MCLK/D4	I/O	1	MCLK/D4	Comp_of_IOR10C	NONE		
IOR10E/FASTRD_N/D3	I/O	1	FASTRD_N/D3	True_of_IOR10F	NONE		
IOR10F/SI/D2	I/O	1	SI/D2	Comp_of_IOR10E	NONE		
IOR10G/SO/D1	I/O	1	SO/D1	True_of_IOR10H	NONE		
IOR10H/SSPI_CS_N/D0	I/O	1	SSPI_CS_N/D0	Comp_of_IOR10G	NONE		
IOR10I/DIN/CLKHOLD_N	I/O	1	DIN/CLKHOLD_N	True_of_IOR10J	NONE		
IOR10J/DOUT/WE_N	I/O	1	DOUT/WE_N	Comp_of_IOR10I	NONE		
IOR11A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR11B	TRUE	32	32
IOR11B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR11A	TRUE	31	31
IOR12A	I/O	1		True_of_IOR12B	NONE		
IOR12B	I/O	1		Comp_of_IOR12A	NONE		
IOR13A	I/O	1		True_of_IOR13B	TRUE		
IOR13B	I/O	1		Comp_of_IOR13A	TRUE		
IOR14A	I/O	1		True_of_IOR14B	NONE		
IOR14B	I/O	1		Comp_of_IOR14A	NONE		
IOR15A	I/O	1		True_of_IOR15B	TRUE		
IOR15B	I/O	1		Comp_of_IOR15A	TRUE		
IOR16A	I/O	1		True_of_IOR16B	NONE		
IOR16B	I/O	1		Comp_of_IOR16A	NONE		
IOR17A	I/O	1		True_of_IOR17B	TRUE		
IOR17B	I/O	1		Comp_of_IOR17A	TRUE		
IOR18A	I/O	1		True_of_IOR18B	NONE		
IOR18B	I/O	1		Comp_of_IOR18A	NONE		
IOR2A	I/O	1		True_of_IOR2B	TRUE		
IOR2B	I/O	1		Comp_of_IOR2A	TRUE		
IOR3A/RPLL_T_in	I/O	1	RPLL_T_in	True_of_IOR3B	NONE	35	35
IOR3B/RPLL_C_in	I/O	1	RPLL_C_in	Comp_of_IOR3A	NONE		
IOR4A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR4B	TRUE		

Note!

[1][2] In package QN48 and QN48E, IOL10B/TCK and GPIO8/TCK share pin 5 and IOL10A/TMS and GPIO11/TMS share pin 7.

[3][4] The configuration pin TDO of GW1NRF-4B is connected to the configuration pin TDI of BLE, forming a JTAG daisy chain.

[5] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
IOR4B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR4A	TRUE		
IOR5A	I/O	1		True_of_IOR5B	NONE		
IOR5B	I/O	1		Comp_of_IOR5A	NONE		
IOR6A	I/O	1		True_of_IOR6B	TRUE		
IOR6B	I/O	1		Comp_of_IOR6A	TRUE		
IOR7A	I/O	1		True_of_IOR7B	NONE		
IOR7B	I/O	1		Comp_of_IOR7A	NONE		
IOR8A	I/O	1		True_of_IOR8B	TRUE		
IOR8B	I/O	1		Comp_of_IOR8A	TRUE		
IOR9A/GCLKT_2	I/O	1	GCLKT_2	True_of_IOR9B	NONE	33	33
IOR9B/GCLKC_2	I/O	1	GCLKC_2	Comp_of_IOR9A	NONE		
IOT12A	I/O	0		True_of_IOT12B	NONE		
IOT12B	I/O	0		Comp_of_IOT12A	NONE		
IOT13A	I/O	0		True_of_IOT13B	NONE		
IOT13B	I/O	0		Comp_of_IOT13A	NONE		
IOT14A	I/O	0		True_of_IOT14B	NONE		
IOT14B	I/O	0		Comp_of_IOT14A	NONE		
IOT15A	I/O	0		True_of_IOT15B	NONE		
IOT15B	I/O	0		Comp_of_IOT15A	NONE		
IOT16A	I/O	0		True_of_IOT16B	NONE	45	45
IOT16B	I/O	0		Comp_of_IOT16A	NONE	44	44
IOT17A	I/O	0		True_of_IOT17B	NONE		
IOT17B	I/O	0		Comp_of_IOT17A	NONE		
IOT18A	I/O	0		True_of_IOT18B	NONE		
IOT18B	I/O	0		Comp_of_IOT18A	NONE		
IOT20A	I/O	0		True_of_IOT20B	NONE		
IOT20B	I/O	0		Comp_of_IOT20A	NONE		
IOT21A	I/O	0		True_of_IOT21B	NONE		
IOT21B	I/O	0		Comp_of_IOT21A	NONE		

Note!

[1][2] In package QN48 and QN48E, IOL10B/TCK and GPIO8/TCK share pin 5 and IOL10A/TMS and GPIO11/TMS share pin 7.

[3][4] The configuration pin TDO of GW1NRF-4B is connected to the configuration pin TDI of BLE, forming a JTAG daisy chain.

[5] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
IOT22A	I/O	0		True_of_IOT22B	NONE		
IOT22B	I/O	0		Comp_of_IOT22A	NONE		
IOT23A	I/O	0		True_of_IOT23B	NONE		
IOT23B	I/O	0		Comp_of_IOT23A	NONE		
IOT24A	I/O	0		True_of_IOT24B	NONE	43	43
IOT24B	I/O	0		Comp_of_IOT24A	NONE	42	42
IOT25A	I/O	0		True_of_IOT25B	NONE		
IOT25B	I/O	0		Comp_of_IOT25A	NONE		
IOT26A	I/O	0		True_of_IOT26B	NONE		
IOT26B	I/O	0		Comp_of_IOT26A	NONE		
IOT27A	I/O	0		True_of_IOT27B	NONE		
IOT27B	I/O	0		Comp_of_IOT27A	NONE		
IOT2A	I/O	0		True_of_IOT2B	NONE		
IOT2B/MODE0	I/O	0	MODE0	Comp_of_IOT2A	NONE	GND[5]	GND[5]
IOT30A	I/O	0		True_of_IOT30B	NONE	41	41
IOT30B	I/O	0		Comp_of_IOT30A	NONE	40	40
IOT31A	I/O	0		True_of_IOT31B	NONE		
IOT31B	I/O	0		Comp_of_IOT31A	NONE		
IOT32A	I/O	0		True_of_IOT32B	NONE		
IOT32B	I/O	0		Comp_of_IOT32A	NONE		
IOT33A	I/O	0		True_of_IOT33B	NONE		
IOT33B	I/O	0		Comp_of_IOT33A	NONE		
IOT34A	I/O	0		True_of_IOT34B	NONE	39	39
IOT34B	I/O	0		Comp_of_IOT34A	NONE		
IOT35A	I/O	0		True_of_IOT35B	NONE		
IOT35B	I/O	0		Comp_of_IOT35A	NONE		
IOT36A	I/O	0		True_of_IOT36B	NONE		
IOT36B	I/O	0		Comp_of_IOT36A	NONE		

Note!

[1][2] In package QN48 and QN48E, IOL10B/TCK and GPIO8/TCK share pin 5 and IOL10A/TMS and GPIO11/TMS share pin 7.

[3][4] The configuration pin TDO of GW1NRF-4B is connected to the configuration pin TDI of BLE, forming a JTAG daisy chain.

[5] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
IOT37A	I/O	0		True_of_IOT37B	NONE		
IOT37B	I/O	0		Comp_of_IOT37A	NONE		
IOT3A/MODE2	I/O	0	MODE2	True_of_IOT3B	NONE	GND[5]	GND[5]
IOT3B/MODE1	I/O	0	MODE1	Comp_of_IOT3A	NONE	GND[5]	GND[5]
IOT4A	I/O	0		True_of_IOT4B	NONE		
IOT4B	I/O	0		Comp_of_IOT4A	NONE		
IOT5A	I/O	0		True_of_IOT5B	NONE		
IOT5B	I/O	0		Comp_of_IOT5A	NONE		
IOT6A	I/O	0		True_of_IOT6B	NONE		
IOT6B	I/O	0		Comp_of_IOT6A	NONE		
IOT7A	I/O	0		True_of_IOT7B	NONE		
IOT7B	I/O	0		Comp_of_IOT7A	NONE		
IOT8A	I/O	0		True_of_IOT8B	NONE		
IOT8B	I/O	0		Comp_of_IOT8A	NONE		
IOT9A	I/O	0		True_of_IOT9B	NONE	47	47
IOT9B	I/O	0		Comp_of_IOT9A	NONE	46	46
VCC	Power	N/A				11	11
VCC	Power	N/A				37	37
VCCIO0/VCCIO3	Power	N/A				1	1
VCCIO1/VCCIO2	Power	N/A				25	25
VCCX	Power	N/A				36	36
VSS	Ground	N/A				2	
VSS	Ground	N/A				26	26
GPIO10/TDI[4]			BLE/TDI				2
GPIO9/TDO			BLE/TDO			4	4
GPIO8/TCK			BLE/TCK			5	5
GPIO11/TMS			BLE/TMS			7	7
XOUT			BLE			9	9

Note!

[1][2] In package QN48 and QN48E, IOL10B/TCK and GPIO8/TCK share pin 5 and IOL10A/TMS and GPIO11/TMS share pin 7.

[3][4] The configuration pin TDO of GW1NRF-4B is connected to the configuration pin TDI of BLE, forming a JTAG daisy chain.

[5] The pin is internally grounded.

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
XIN			BLE			10	10
ANT			BLE			12	12
VBAT2			BLE			13	13
ENABLE			BLE			14	14
LF_XIN			BLE			15	15
LF_XOUT			BLE			16	16
MCUVCC			BLE			27	27
VCCGPIO			BLE			28	28
VBAT1			BLE			29	29
SW_DCDC			BLE			30	30
GPIO5			BLE			34	34
GPIO6			BLE			38	38
GPIO7			BLE			48	48

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
BANK3 True LVDS Pair							
IOL11A/GCLKT_6	I/O	3	GCLKT_6	True_of_IOL11B	TRUE	8	
IOL11B/GCLKC_6	I/O	3	GCLKC_6	Comp_of_IOL11A	TRUE		
IOL13A	I/O	3		True_of_IOL13B	TRUE		
IOL13B	I/O	3		Comp_of_IOL13A	TRUE		
IOL15A	I/O	3		True_of_IOL15B	TRUE		
IOL15B	I/O	3		Comp_of_IOL15A	TRUE		
IOL17A	I/O	3		True_of_IOL17B	TRUE		
IOL17B	I/O	3		Comp_of_IOL17A	TRUE		
IOL2A	I/O	3		True_of_IOL2B	TRUE		
IOL2B	I/O	3		Comp_of_IOL2A	TRUE		
IOL4A/LPLL_T_fb	I/O	3	LPLL_T_fb	True_of_IOL4B	TRUE		
IOL4B/LPLL_C_fb	I/O	3	LPLL_C_fb	Comp_of_IOL4A	TRUE		
IOL6A	I/O	3		True_of_IOL6B	TRUE		
IOL6B	I/O	3		Comp_of_IOL6A	TRUE		
IOL8A	I/O	3		True_of_IOL8B	TRUE		
IOL8B	I/O	3		Comp_of_IOL8A	TRUE		
BANK2 True LVDS Pair							
IOB12A	I/O	2		True_of_IOB12B	TRUE		
IOB12B	I/O	2		Comp_of_IOB12A	TRUE		
IOB14A	I/O	2		True_of_IOB14B	TRUE		
IOB14B	I/O	2		Comp_of_IOB14A	TRUE		
IOB16A	I/O	2		True_of_IOB16B	TRUE		
IOB16B	I/O	2		Comp_of_IOB16A	TRUE		
IOB18A	I/O	2		True_of_IOB18B	TRUE		
IOB18B	I/O	2		Comp_of_IOB18A	TRUE		
IOB20A/GCLKT_4	I/O	2	GCLKT_4	True_of_IOB20B	TRUE	19	19
IOB20B/GCLKC_4	I/O	2	GCLKC_4	Comp_of_IOB20A	TRUE	20	20
IOB22A	I/O	2		True_of_IOB22B	TRUE		
IOB22B	I/O	2		Comp_of_IOB22A	TRUE		
IOB24A	I/O	2		True_of_IOB24B	TRUE		
IOB24B	I/O	2		Comp_of_IOB24A	TRUE		

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
IOB26A	I/O	2		True_of_IOB26B	TRUE	21	21
IOB26B	I/O	2		Comp_of_IOB26A	TRUE	22	22
IOB2A	I/O	2		True_of_IOB2B	TRUE		
IOB2B	I/O	2		Comp_of_IOB2A	TRUE		
IOB30A	I/O	2		True_of_IOB30B	TRUE		
IOB30B	I/O	2		Comp_of_IOB30A	TRUE		
IOB32A	I/O	2		True_of_IOB32B	TRUE	23	23
IOB32B	I/O	2		Comp_of_IOB32A	TRUE	24	24
IOB34A	I/O	2		True_of_IOB34B	TRUE		
IOB34B	I/O	2		Comp_of_IOB34A	TRUE		
IOB36A	I/O	2		True_of_IOB36B	TRUE		
IOB36B	I/O	2		Comp_of_IOB36A	TRUE		
IOB4A	I/O	2		True_of_IOB4B	TRUE		
IOB4B	I/O	2		Comp_of_IOB4A	TRUE		
IOB6A	I/O	2		True_of_IOB6B	TRUE		
IOB6B	I/O	2		Comp_of_IOB6A	TRUE		
IOB8A	I/O	2		True_of_IOB8B	TRUE		
IOB8B	I/O	2		Comp_of_IOB8A	TRUE		
BANK1 True LVDS Pair							
IOR11A/GCLKT_3	I/O	1	GCLKT_3	True_of_IOR11B	TRUE	32	32
IOR11B/GCLKC_3	I/O	1	GCLKC_3	Comp_of_IOR11A	TRUE	31	31
IOR13A	I/O	1		True_of_IOR13B	TRUE		
IOR13B	I/O	1		Comp_of_IOR13A	TRUE		
IOR15A	I/O	1		True_of_IOR15B	TRUE		
IOR15B	I/O	1		Comp_of_IOR15A	TRUE		
IOR17A	I/O	1		True_of_IOR17B	TRUE		
IOR17B	I/O	1		Comp_of_IOR17A	TRUE		
IOR2A	I/O	1		True_of_IOR2B	TRUE		
IOR2B	I/O	1		Comp_of_IOR2A	TRUE		
IOR4A/RPLL_T_fb	I/O	1	RPLL_T_fb	True_of_IOR4B	TRUE		
IOR4B/RPLL_C_fb	I/O	1	RPLL_C_fb	Comp_of_IOR4A	TRUE		
IOR6A	I/O	1		True_of_IOR6B	TRUE		

Pin Name	Function	BANK	Configuration Function	Differential Pair	LVDS	QN48	QN48E
IOR6B	I/O	1		Comp_of_IOR6A	TRUE		
IOR8A	I/O	1		True_of_IOR8B	TRUE		
IOR8B	I/O	1		Comp_of_IOR8A	TRUE		