

Gowin USB 1.1 SoftPHY IP

User Guide

IPUG759-1.1E, 04/09/2021

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Revision History

| Date | Version | Description |
|------------|---------|--|
| 01/06/2021 | 1.0E | Initial version published. |
| 04/09/2021 | 1.1E | Chapter 3 Functional Description modified. |

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1 About This Guide

1.1 Purpose

The purpose of Gowin USB 1.1 SoftPHY User Guide is to help you learn the features and usage of Gowin USB 1.1 by providing an overview of the signal description, functional description and interface configuration.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at <u>www.gowinsemi.com</u>:

- 1. <u>DS100</u>, GW1N series of FPGA Products Data Sheet
- 2. DS117, GW1NR series of FPGA Products Data Sheet
- 3. <u>DS891</u>, GW1NRF series of FPGA Products Data Sheet
- 4. <u>DS821</u>, GW1NS series of FPGA Products Data Sheet
- 5. <u>DS871</u>, GW1NSE series of FPGA Products Data Sheet
- 6. <u>DS881</u>, GW1NSER series of FPGA Products Data Sheet
- 7. DS861, GW1NSR series of FPGA Products Data Sheet
- 8. DS102, GW2A series of FPGA Products Data Sheet
- 9. <u>DS226</u>, GW2AR series of FPGA Products Data Sheet
- 10. SUG100, Gowin Software User Guide

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

| Terminology and Abbreviations | Meaning |
|-------------------------------|---|
| IP | Intellectual Property |
| USB | General Serial Bus |
| UTMI | USB 2.0 Transceiver Macrocell Interface |
| HS | High Speed |
| FS | Full Speed |
| LS | Low Speed |

Table 1-1 Terminology and Abbreviations

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Introduction

2.1 Overview

Gowin USB 1.1 SoftPHY IP is a USB physical layer transceiver that can support data reception and transmission at full speed (12Mbps) or low speed (1.5Mbps).

2.2 Features

The features of USB 1.1 SoftPHY IP include:

- Supports Full Speed Mode (12Mbps) and Low Speed Mode (1.5Mbps);
- Supports data serial and parallel conversion;
- Supports bit stuffing and extraction;
- Supports NRZI encoding and decoding;
- Supports UTMI interface.

3 Functional Description

3.1 USB 1.1 SoftPHY

In the RX direction, after USB serial data goes through the modules including: CDR, NRZI decoding, bit extraction, data shifting, the realized USB RX data is received, and the received data goes through the UTMI interface to send to the upper module. In the TX direction, after receiving the transmit data, the USB serial data goes through the modules including: data shifting, bit filling, NRZI encoding to generate the serial TX data stream.



Figure 3-1 SoftPHY Block Diagram



Mode (1.5Mbps); When USB 1.1 SoftPHY is used as the master device, a 15K pull-down resistor needs to be connected to Data+ and Data-.

Figure 3-2 USB Master Device Interface Implementation



When USB 1.1 SoftPHY is used as the slave device in full speed, a 1.5K pull-down resistor needs to be connected to Data+.

Figure 3-3 USB Slave Device Interface Implementation



When USB 1.1 SoftPHY is used as the slave device in low speed, a 1.5K pull-down resistor needs to be connected to Data-.





4 Signal Description

4.1 Signal Description

A description of signals is as shown in Table 4-1.

| No. | Signal Name | I/O | Data Width | Description | Remarks |
|--------------|-------------------|-----|------------|---|---------|
| 1 | clk_i | 1 | 1 | Input clock signal | |
| | | | | (24MHz/48MHz/60MHz) | |
| 2 | rst i | 1 | 1 | Asynchronous reset signal resets the | |
| | | - | | state machine inside of PHY. | |
| 3 | utmi_data_out_i | Ι | 8 | Data input, 8 bit parallel send data bus. | |
| 4 | utmi_txvalid_i | Ι | 1 | Transmit data is valid, active-high. | |
| | | | | Operation mode selection signal: | |
| | | | | • 2'b00: Normal | |
| | | | | • 2'b01: No driver | |
| <i>_</i> | utmi opmodo i | | 2 | • 2'b10: Disable bit stuffing and | |
| 5 | utmi_opmode_i | 1 | 2 | NRZI encoding | |
| | | | | 2'b11: Operation of not | |
| | | | | automatically generating start and | |
| | | | | end signals | |
| | | | | Transmit mode selection signal: | |
| | | | | • 2'b00: HS transmission (Not | |
| 0 | | | | supported) | |
| 6 | utmi_xcvrselect_l | | 2 | • 2'b01: FS transmission | |
| | | | | • 2'b10: LS transmission | |
| | | | | • 2'b11: Reserved | |
| | | | | Termination selection: | |
| 7 | | . | 4 | • 1' b0: HS termination enable (Not | |
| [′] | | | | supported) | |
| | | | | • 1' b1: FS/LS termination enable | |

Table 4-1 Signals Description

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| No. | Signal Name | I/O | Data Width | Description | Remarks |
|-----|------------------|-----|------------|--|---------|
| Q | utmi data in o | | 8 | Data Output, 8 bits parallel data | |
| 0 | | 0 | 0 | receive bus. | |
| | | | | Transmit data ready completed signal, | |
| 9 | utmi_txready_o | 0 | 1 | indicating that PHY can receive this | |
| | | | | data. | |
| | | | | Receive data activation indicates that | |
| 10 | utmi_rxactive_o | 0 | 1 | the receive state machines detects the | |
| | | | | SYNC signal and starts receiving data. | |
| 11 | utmi_rxvalid_o | 0 | 1 | Receive data is valid, active-high. | |
| 12 | utmi rvorror o | 0 | 1 | Receive data error, active-high | |
| 12 | | 0 | 1 | indicates receive error. | |
| | | | | Line status of receive: DM DP | |
| | | | | • 2'b00: SE0 | |
| 13 | utmi_linestate_o | 0 | 2 | • 2'b01: "J" | |
| | | | | • 2'b10: "K" | |
| | | | | • 2'b11: SE1 | |
| 14 | usb_dp_io | I/O | 1 | USB data signal Data+ | |
| 15 | usb_dn_io | I/O | 1 | USB data signal Data- | |

4.2 Parameter Configuration Option

Gowin USB 1.1 SoftPHY IP paremeter configuration is shown in Table 4-2.

Table 4-2 Configuration Option

| Option | Description |
|-----------------|---|
| Clock Frequency | Working clock frequency setting includes 24MHz, 48MHz |
| | and 60MHz. |

5 Interface Configuration

Select "Tools" in the Gowin software interface , and it can start the IP Core Generator tool, call and configure USB 1.1 SoftPHY.

1. Open IP Core Generator

After creating the project, you can click the "Tools" tab in the upper left, select and open the IP Core Generator via the drop-down list, as shown in Figure 5-1.

Figure 5-1 IP Core Generator

| The fair from th | W COWIN POA Designer - (Design Summary) | | | | | | |
|--|--|-------------------------------|-----------------|--------------------------------------|----------------------------|---|--------------|
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| Console Message | % | | | | | | |
| | Console Message | | | | | | |

2. Open USB 1.1 SoftPHY IP Core

Select "Soft IP Core > Interface and Interconnect > USB 1.1 IP", as shown in Figure 5-2. Double click to open the configuration interface.



Figure 5-2 Open USB 1.1 SoftPHY IP Core

3. USB 1.1 SoftPHY IP Core Configuration Interface

Figure 5-3 shows the USB 1.1 SoftPHY IP core configuration interface. The interface diagram is on the left. Options are on the right.

- You can configure the file name in File Name;
- You can configure the top module name in Module Name;
- You can configure the speed mode, the power supply mode, the endpoint transmission type, etc. in Options.

Figure 5-3 USB 1.1 SoftPHY IP Configuration Interface

| | General | | | | |
|--|-------------|--------------------------------------|-------------------------------------|-----------------------|--|
| | Device: | GW1NSR-4C | Part Number: | GW1NSR-LV4CMG64PC7/I6 | |
| | Create In: | C:\Users\Administrator\Documents\fpg | ja_project\src\usb | _softphy | |
| | File Name: | usb_softphy | Module Name: | USB_SoftPHY_Top | |
| | Language: | Verilog | Synthesis Tool: | GowinSynthesis | |
| elk i utmidata in of701 🗕 | Options | | | | |
| nati utmitoreadu o utmitoreadu o | Clock Frequ | uency: 60MHz - n Confi 24MHz | | | |
| utmi data out il701 utmi nvactive o 🛨 | ☑ Disabl | 48MHz e I/O Ir <mark>60MHz</mark> | | | |
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