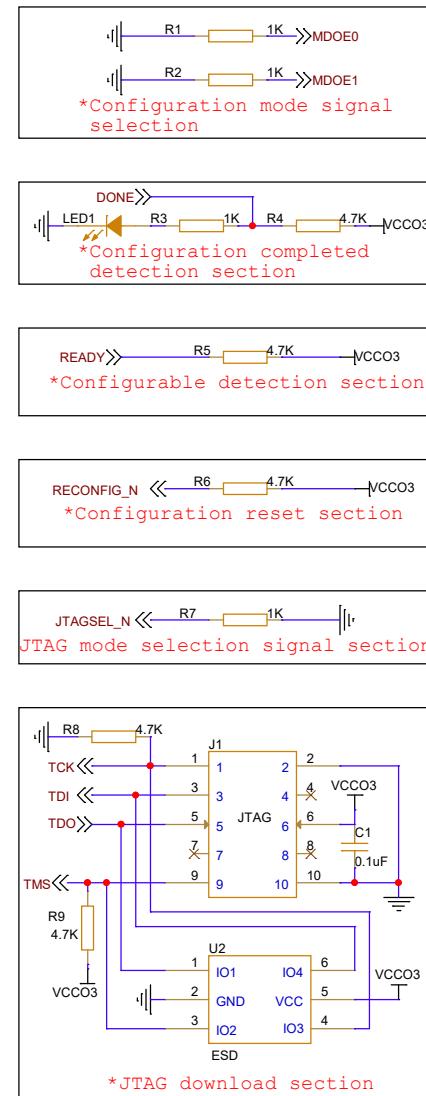


Notes

- NOTES:**

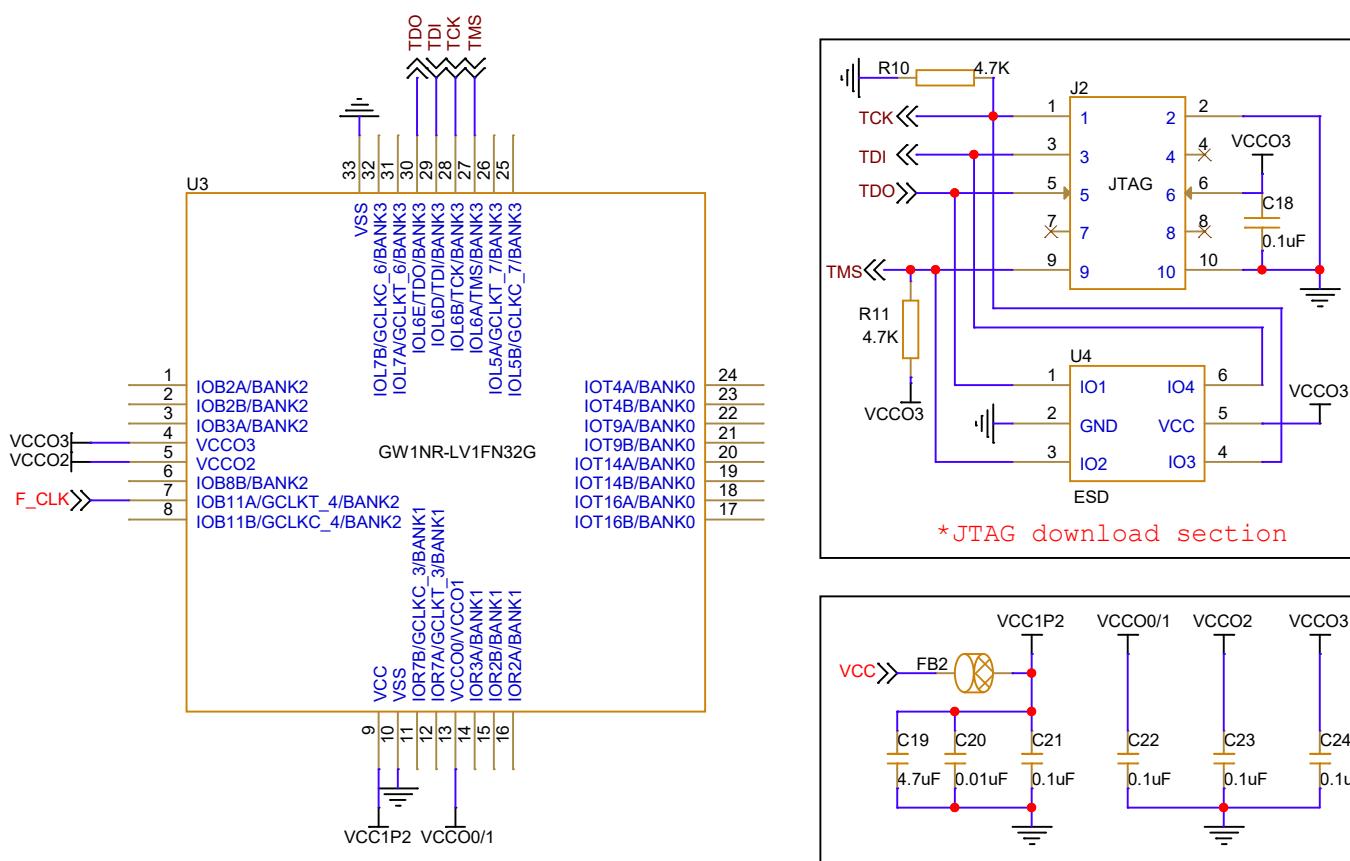
 - 1.F_{CLK} signal is an external input clock signal.
It is recommended that F_{CLK} signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



*JTAG download section

Title		GOWIN Minimum System Diagram		
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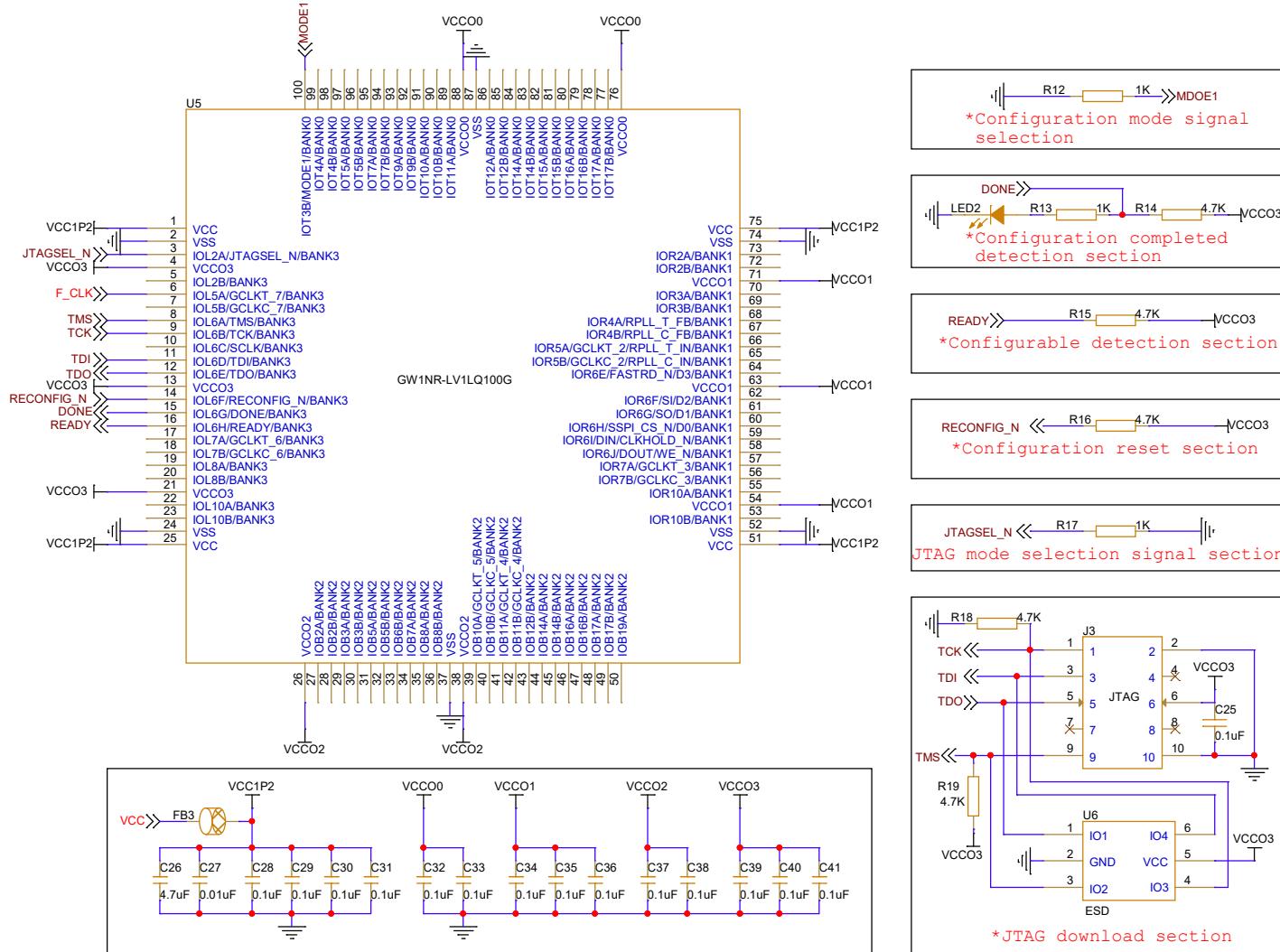
GW1NR-LV1FN32G



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

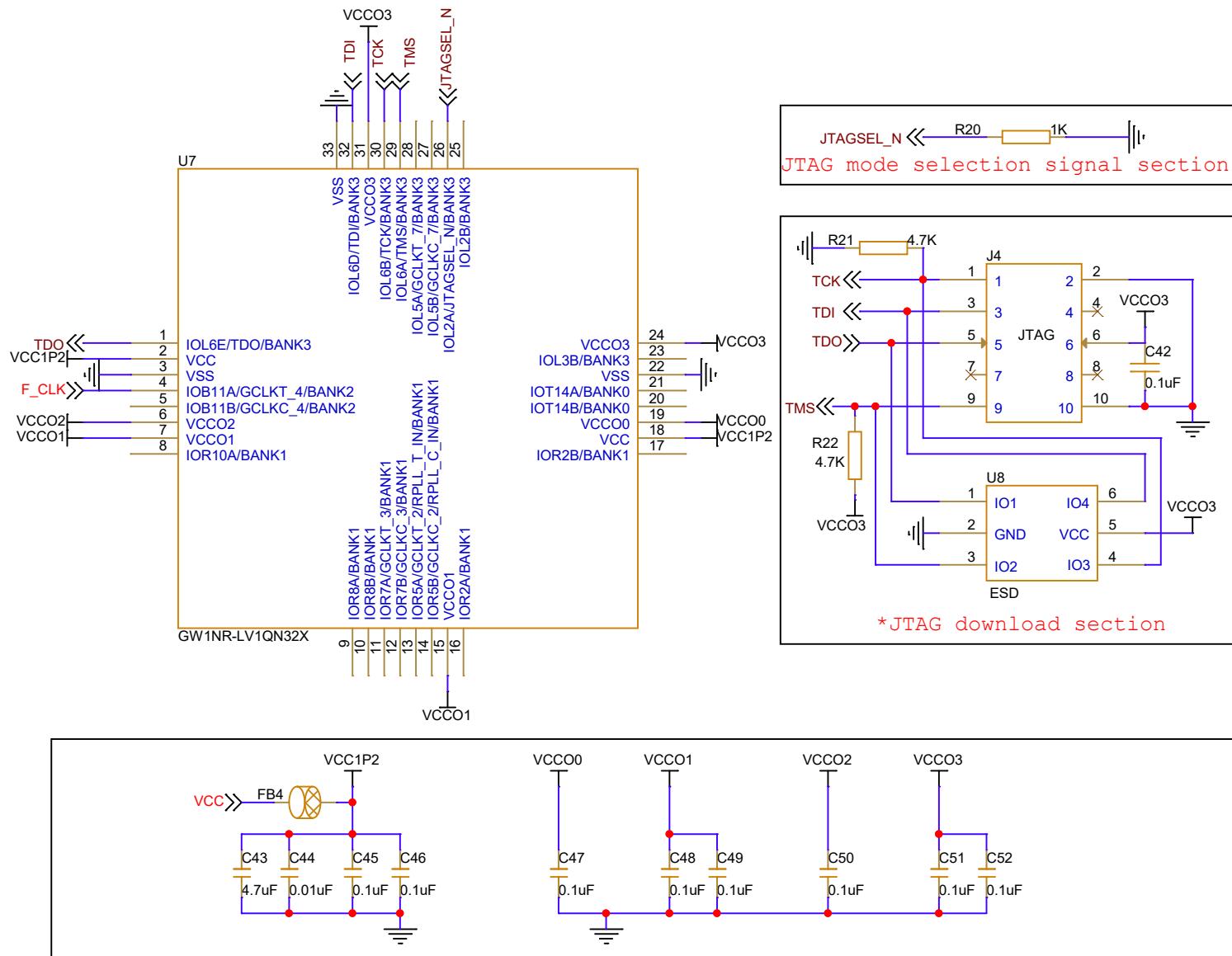
Title	
GOWIN Minimum System Diagram	
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Title	
GOWIN Minimum System Diagram	
Size	Document Number
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GW1NR-LV1QN32X

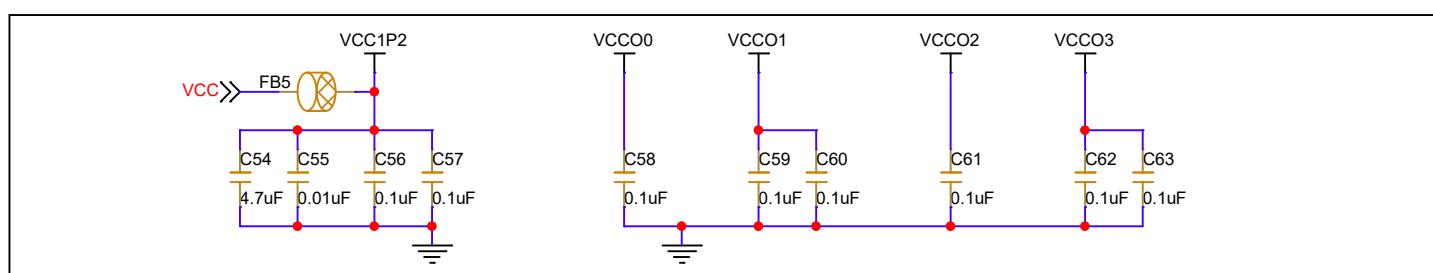
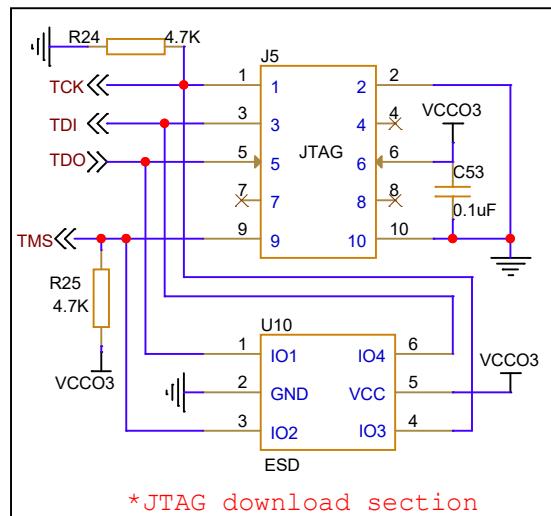
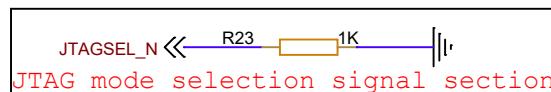
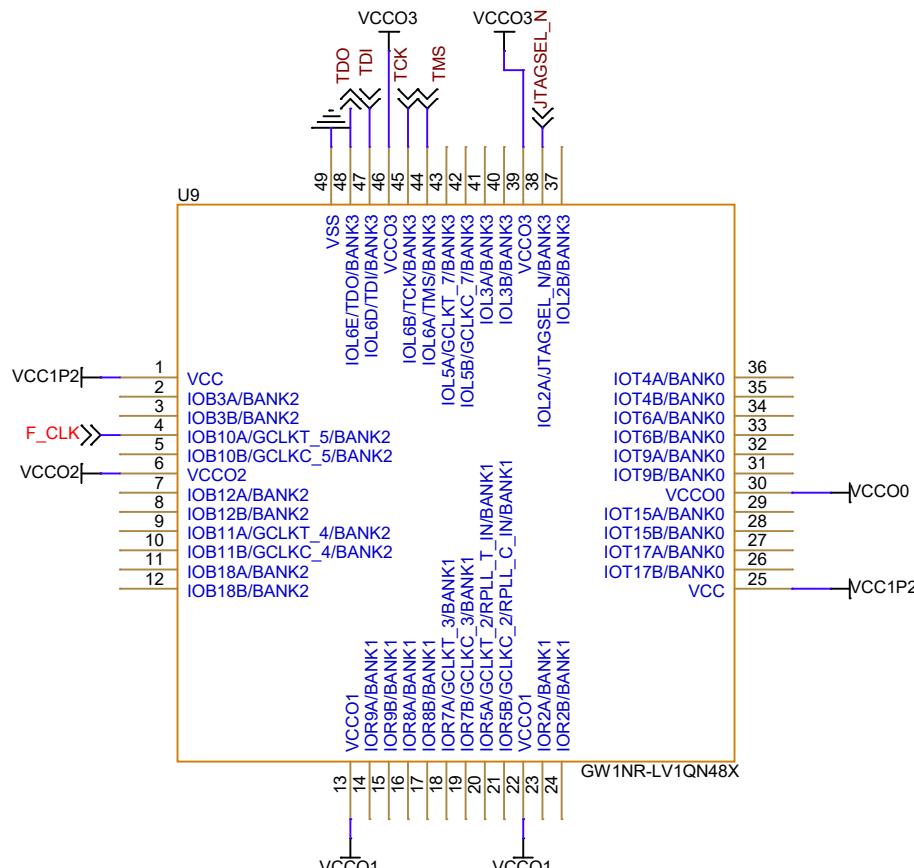


Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
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GW1NR-LV1QN48X



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
Size A4 Document Number GW1NR-LV1QN48X	
Date:	Rev 2.1
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