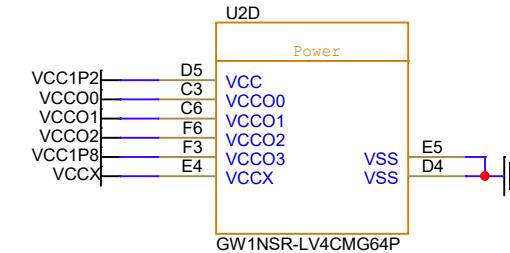
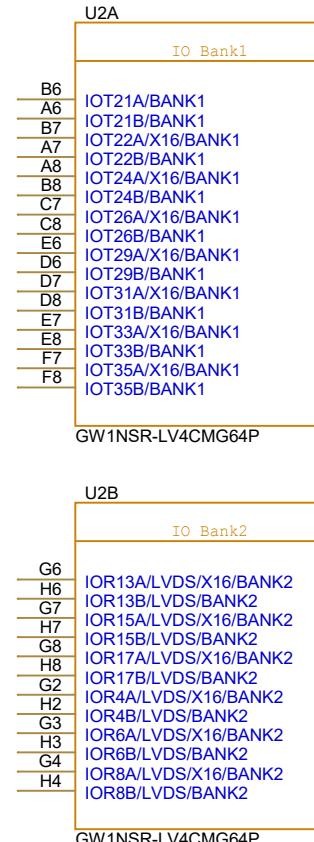
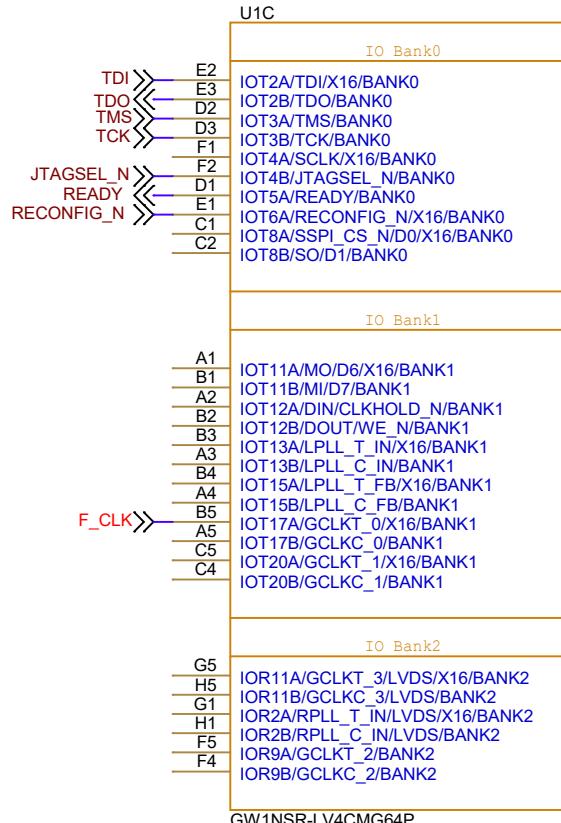
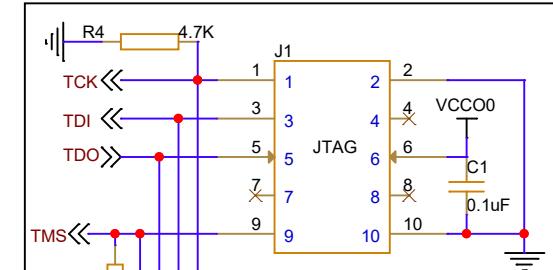


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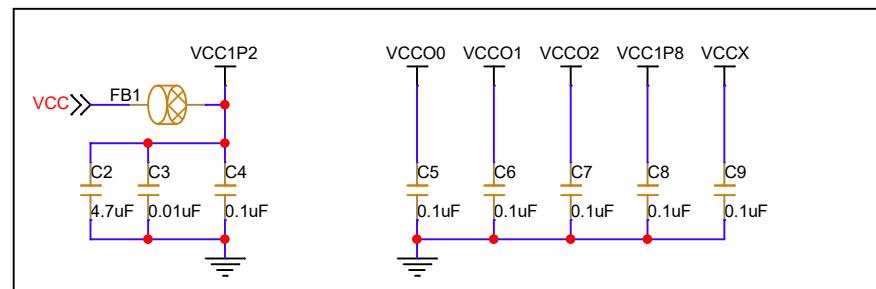
READY \gg R1 4.7K \rightarrow VCC00
***Configurable detection section**

RECONFIG_N \ll R2 4.7K \rightarrow VCC00
***Configuration reset section**

JTAGSEL_N \ll R3 1K \rightarrow I_L
JTAG mode selection signal section



*** JTAG download section**



Notes:

1. F_CLK signal is an external input clock signal.

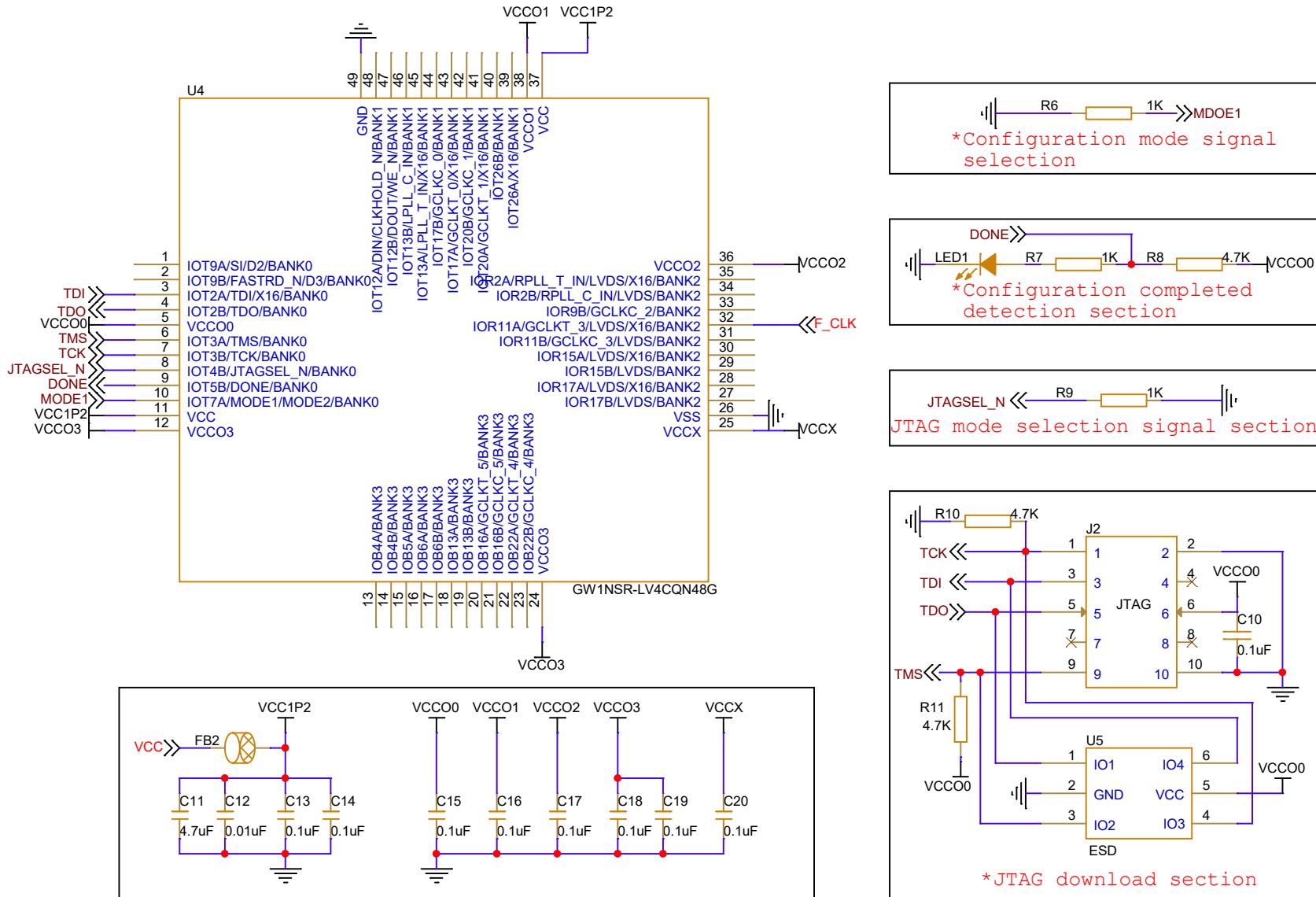
It is recommended that F CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

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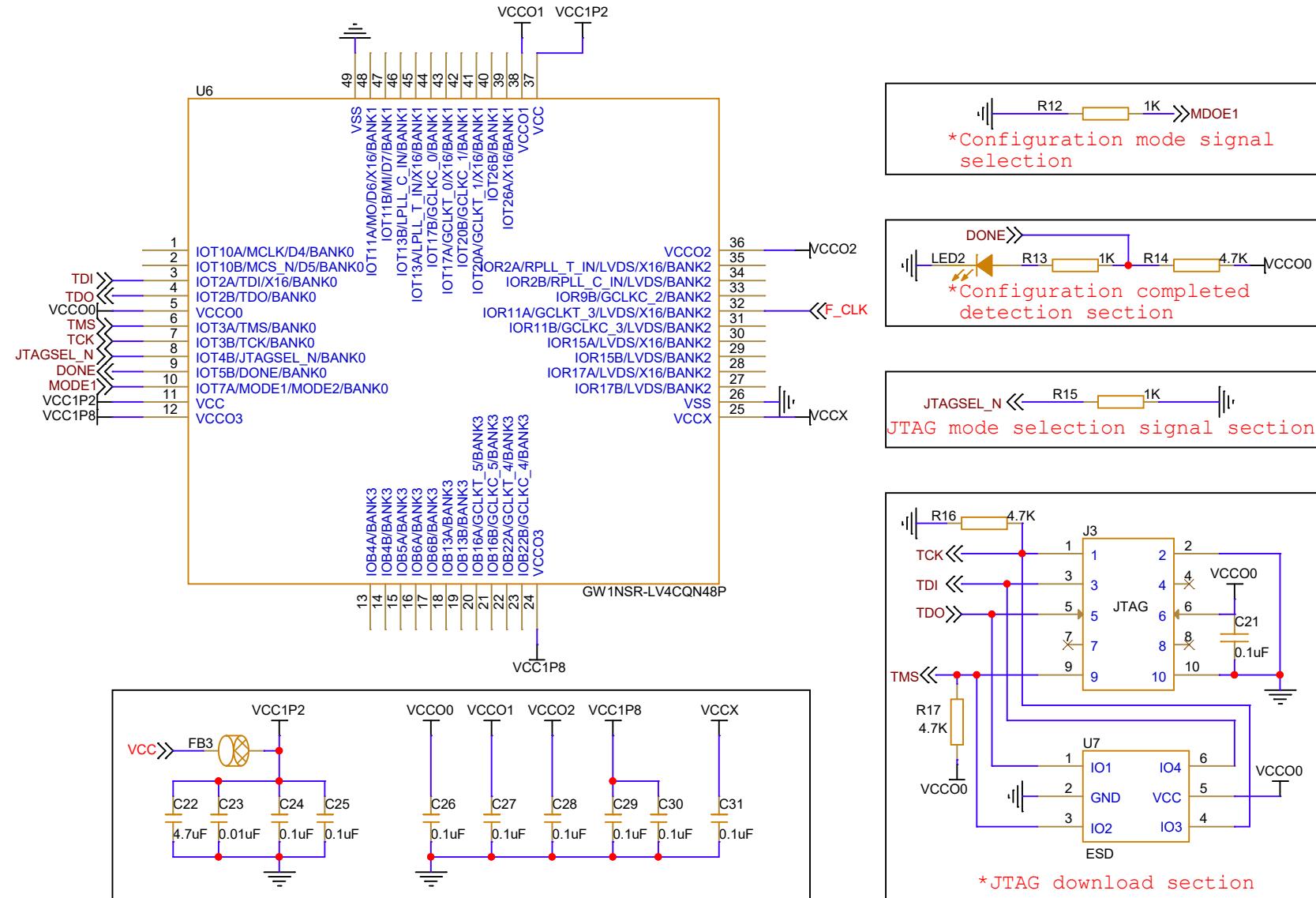
Date: Wednesday, April 10, 2024

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**Notes:**

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

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Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title GOWIN Minimum System Diagram

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Date: Wednesday, April 10, 2024

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