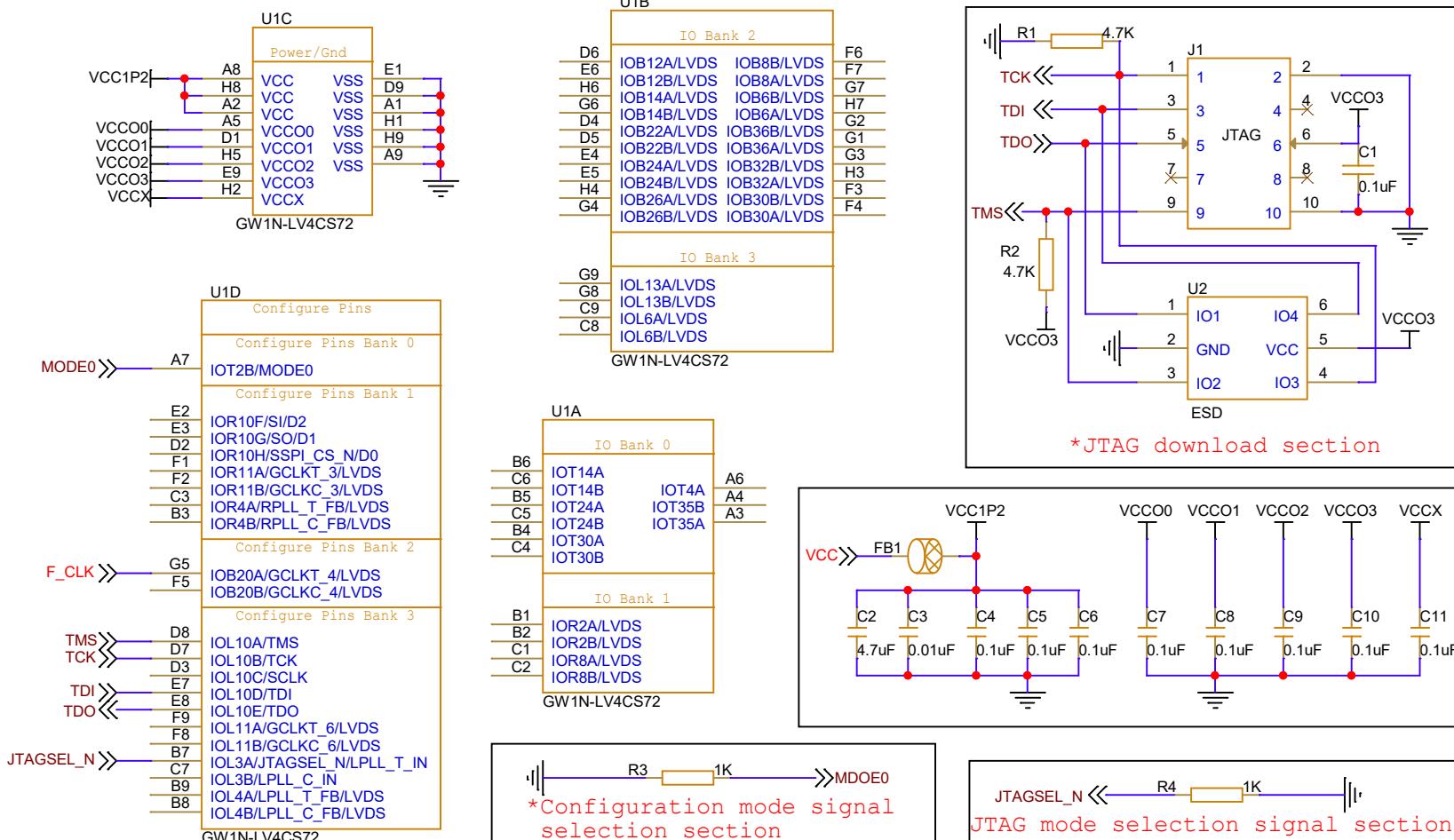


GW1N-LV4CS72



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

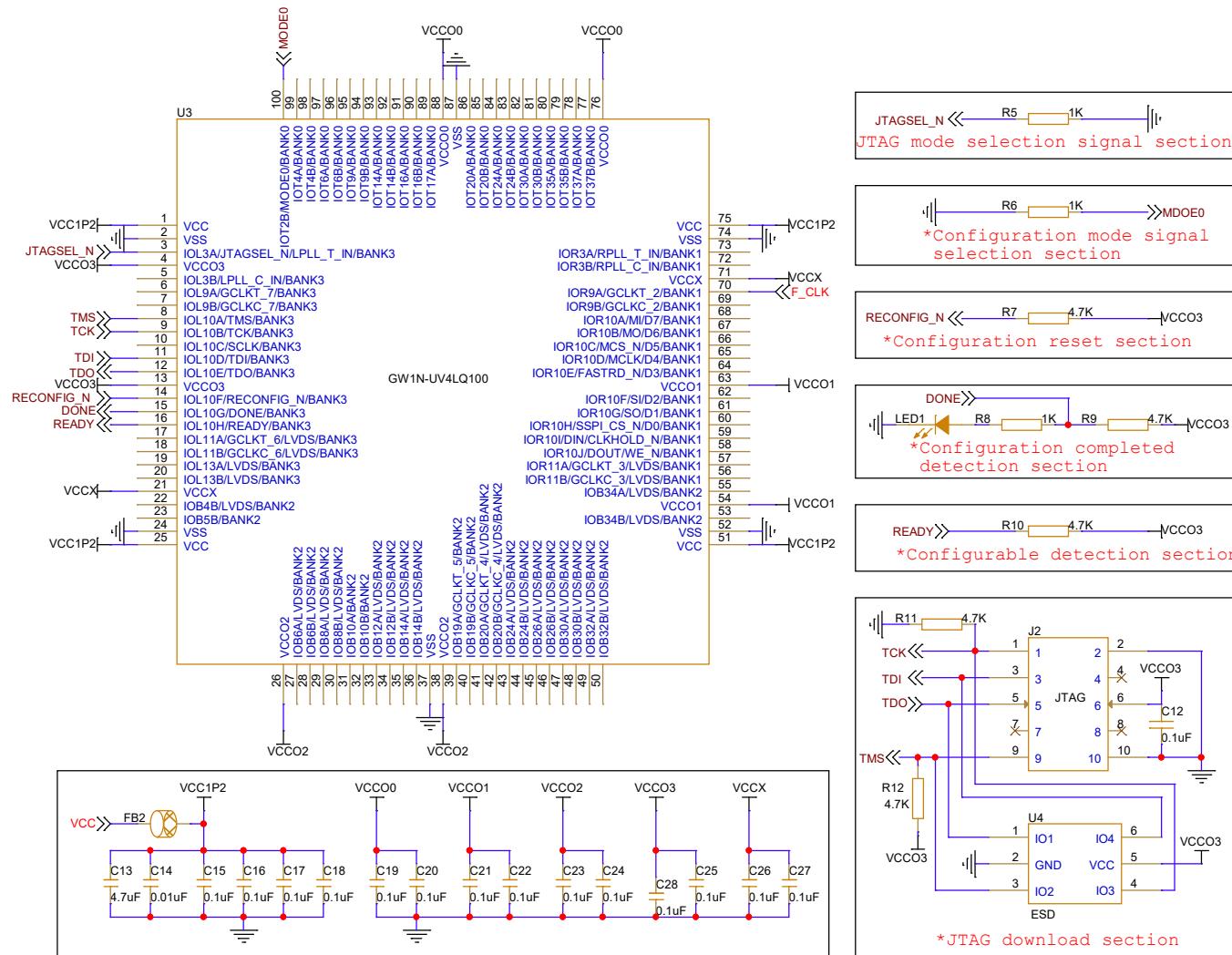
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Size: A4 Document Number: GW1N-LV4CS72

Rev: 2.1

Date: Tuesday, April 09, 2024

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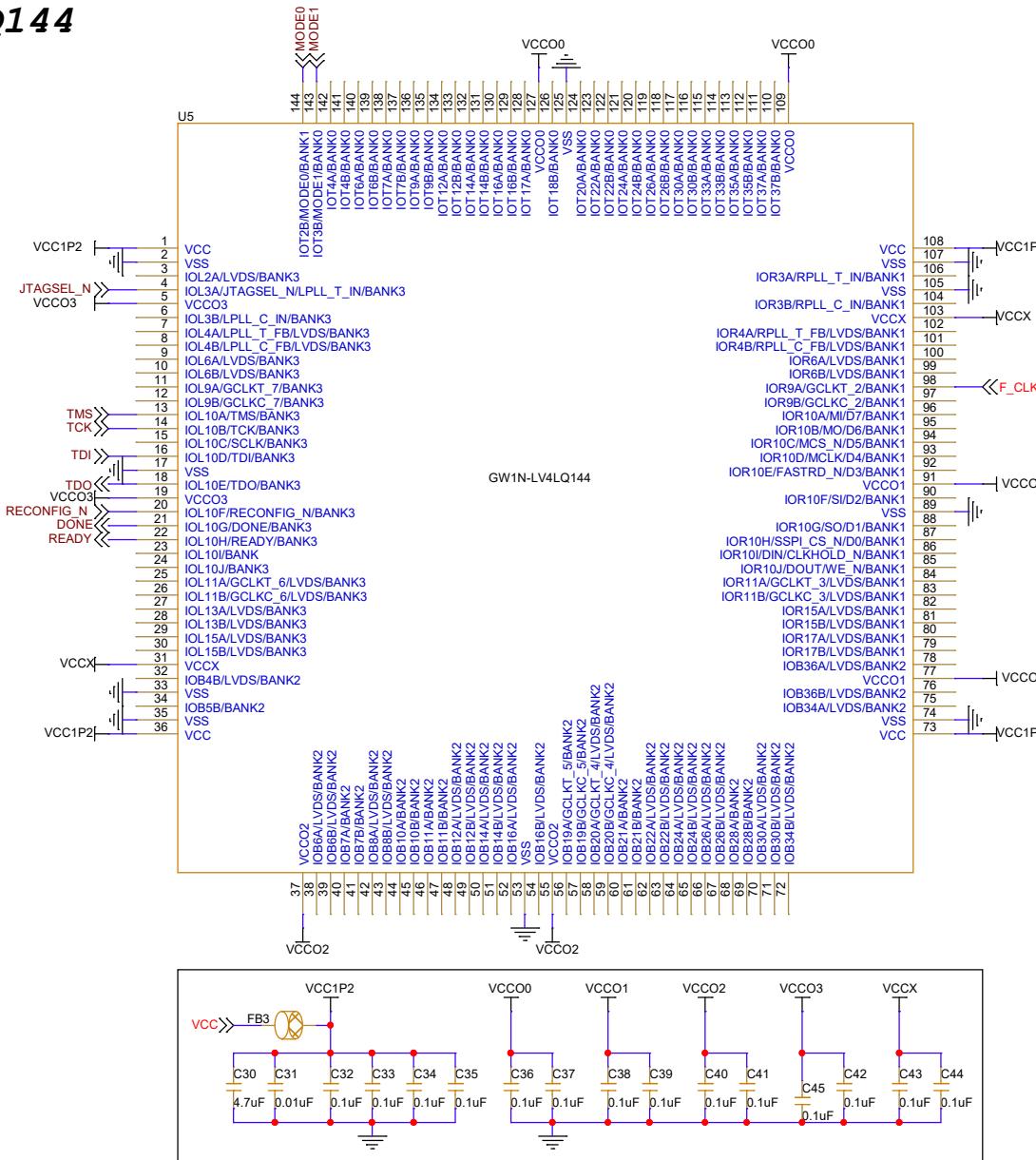
Notes:

1. F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size B	Document Number GW1N-LV4LQ100
Rev 2.1	Date: Tuesday, April 09, 2024

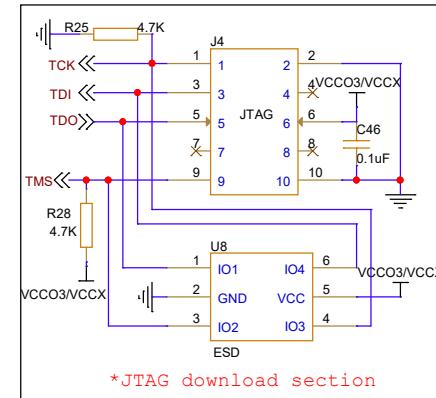
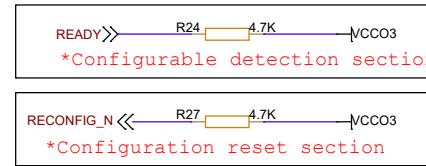
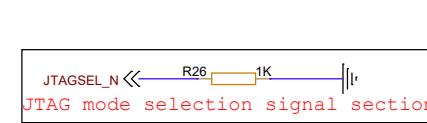
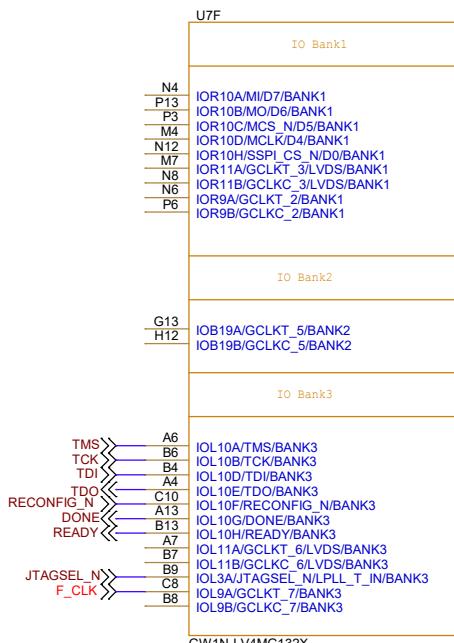
**Notes:**

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title: GOWIN Minimum System Diagram

Size: B Document Number: GW1N-LV4LQ144

Rev: 2.1



Notes:

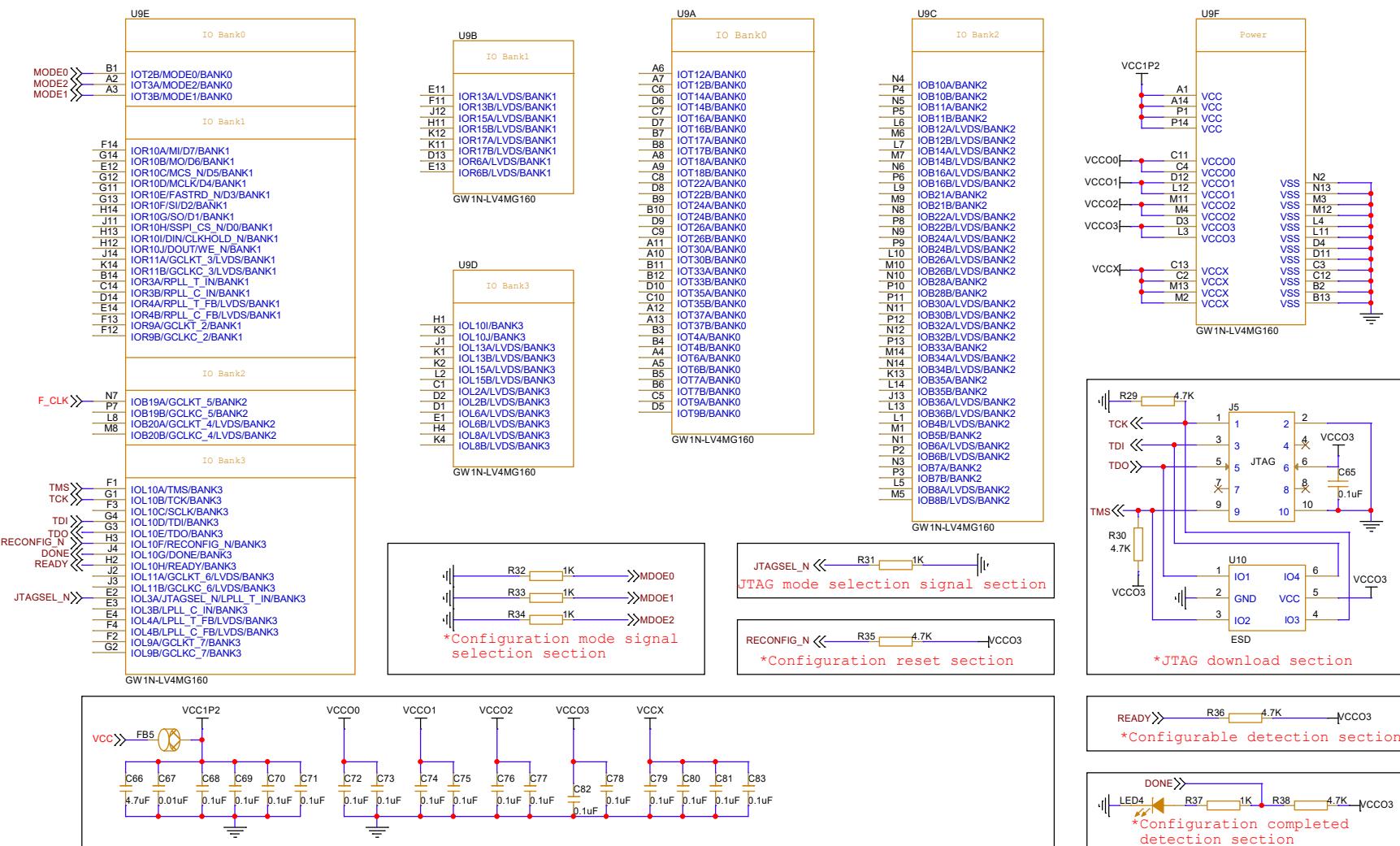
1. F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV4MG132X	2.1

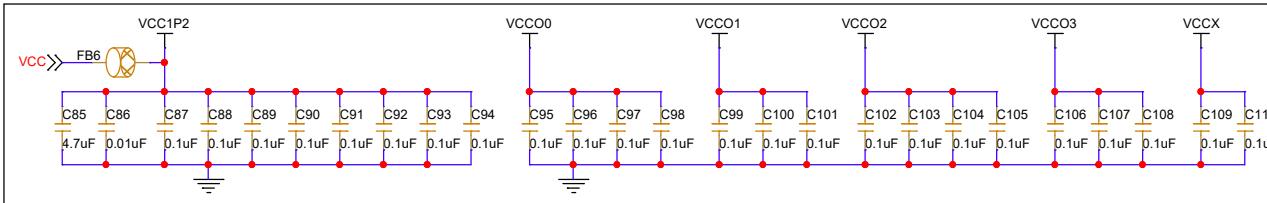
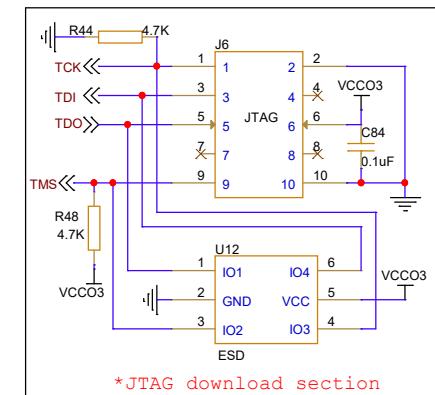
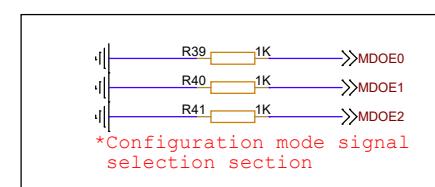
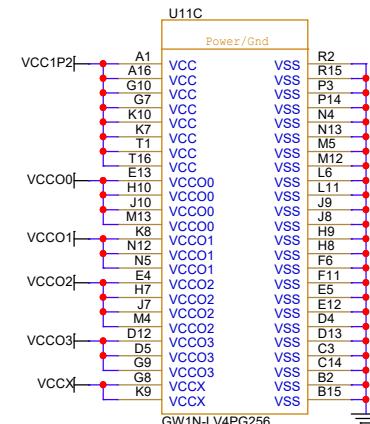
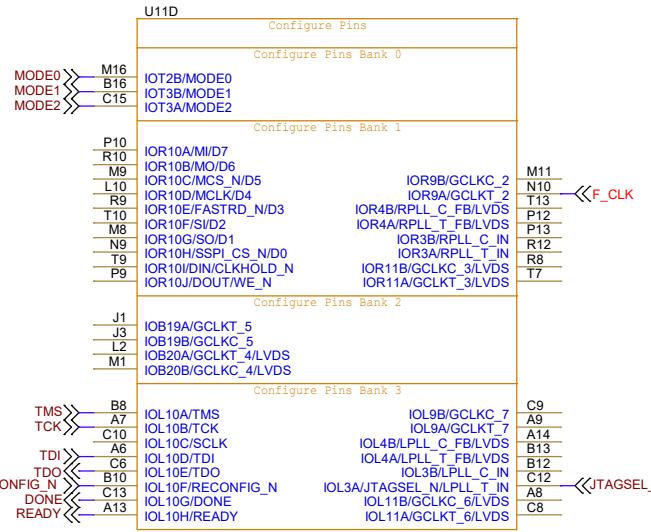
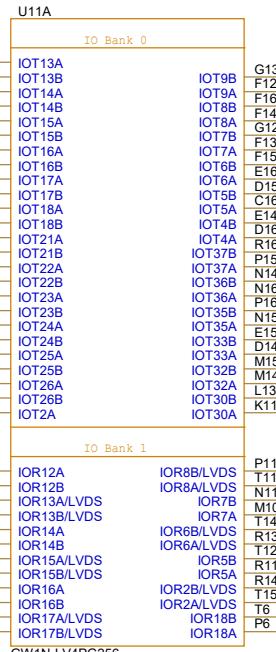
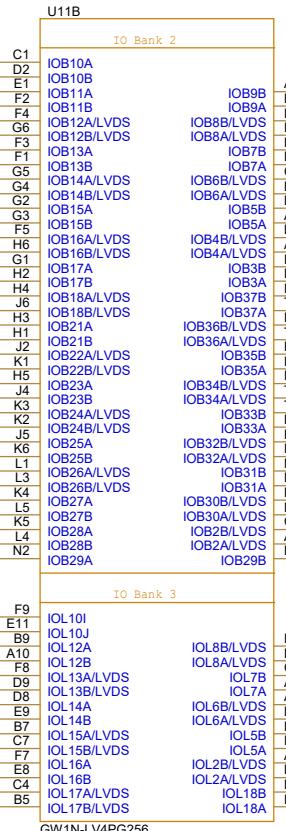
Date: Tuesday, April 09, 2024 Sheet 4 of 22



Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		GOWIN Minimum System Diagram		
Size A3	Document Number GW1-NV4MG160		Rev 2.1	
Date:	Tuesday, April 09, 2024		Sheet 5	of 22

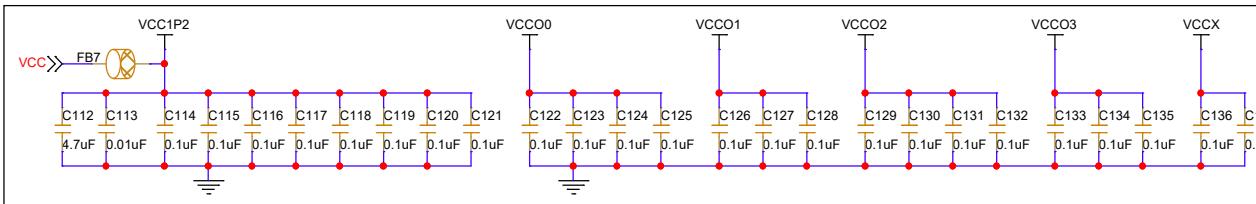
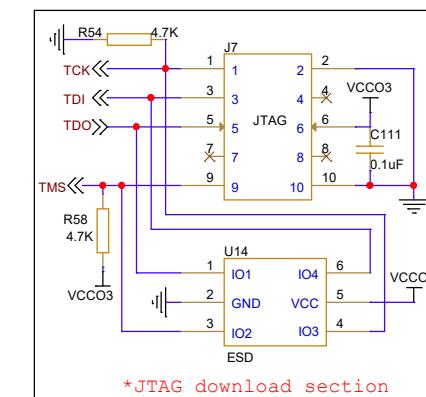
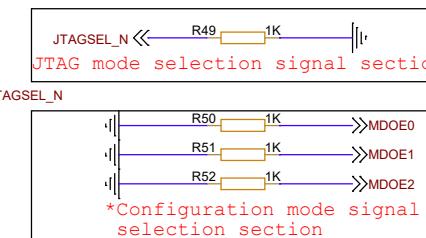
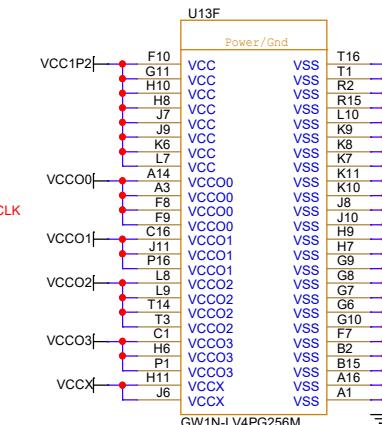
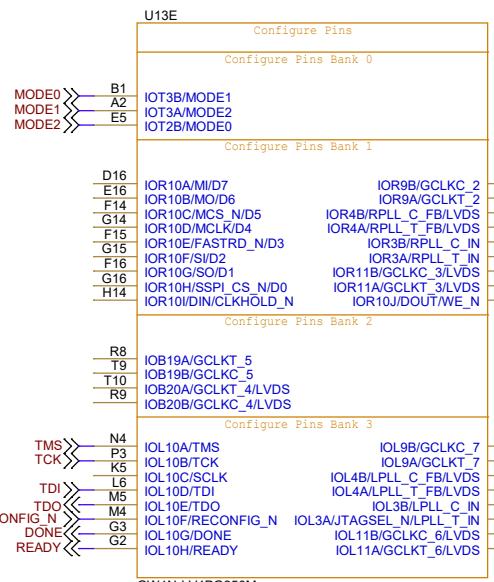
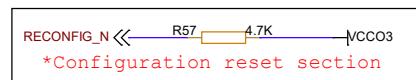
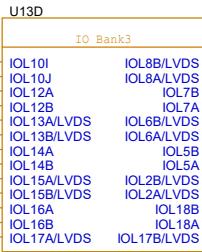
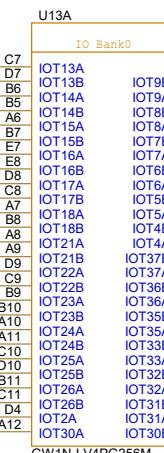
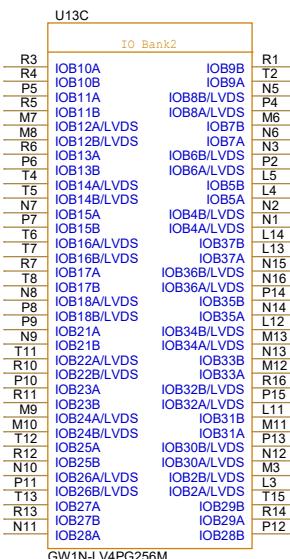


Notes:

1. F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size	Document Number
B	GW1N-LV4PG256
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Date:	Tuesday, April 09, 2024
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GW1N-LV4PG256M



Notes:

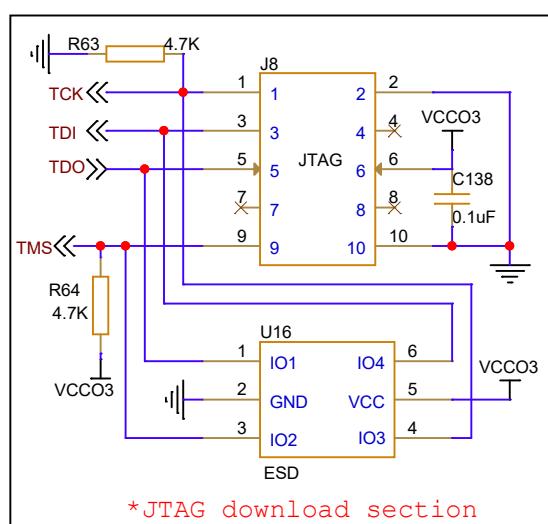
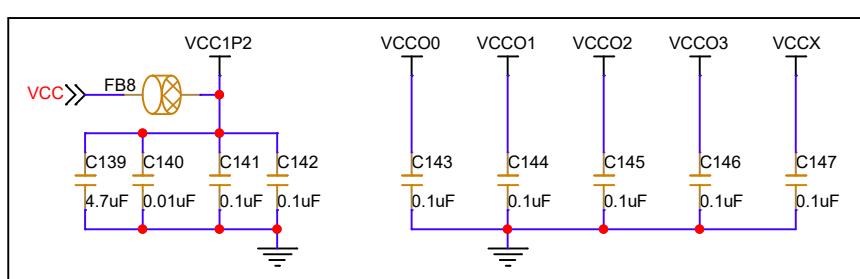
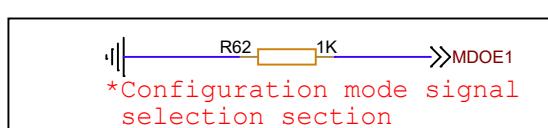
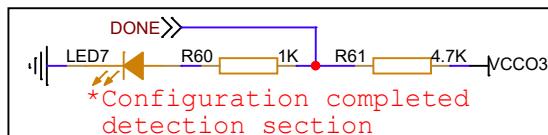
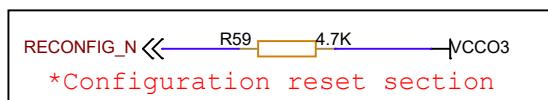
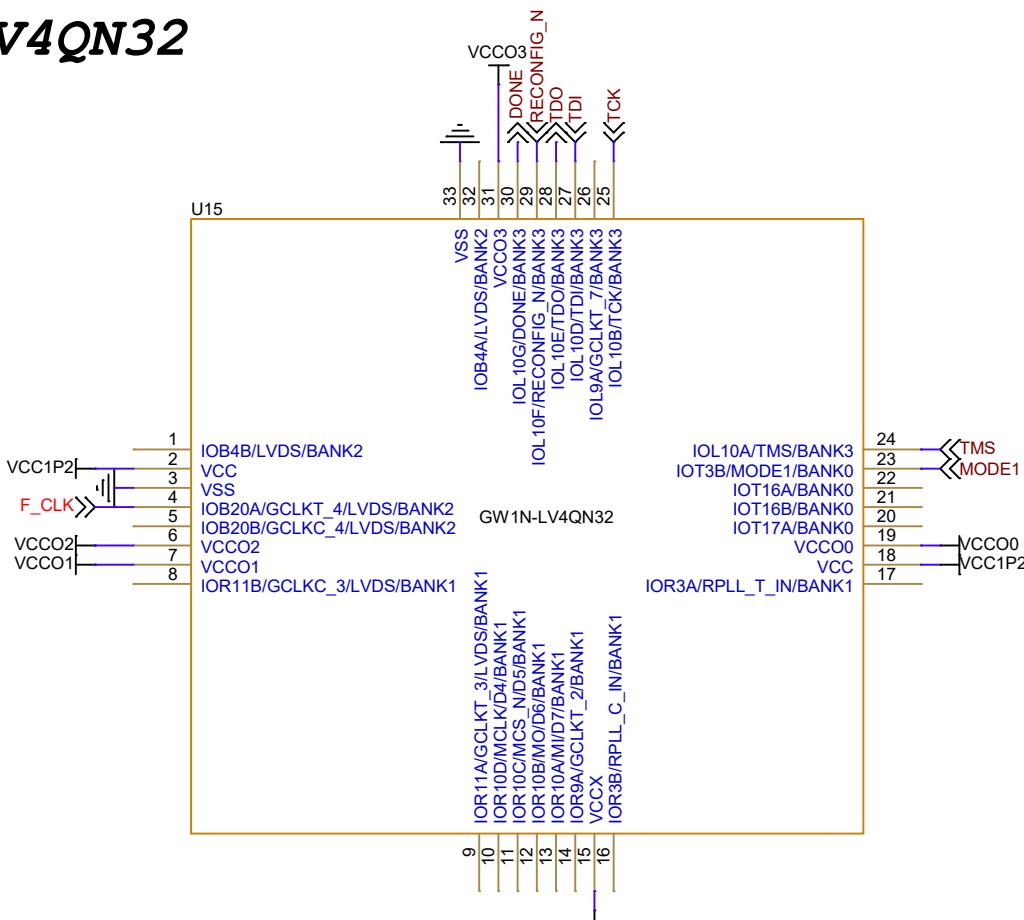
- Notes:

 - 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number GW1N-LV4PG256M	Rev 2.1

GW1N-LV4QN32

5 4 3 2 1



Notes:

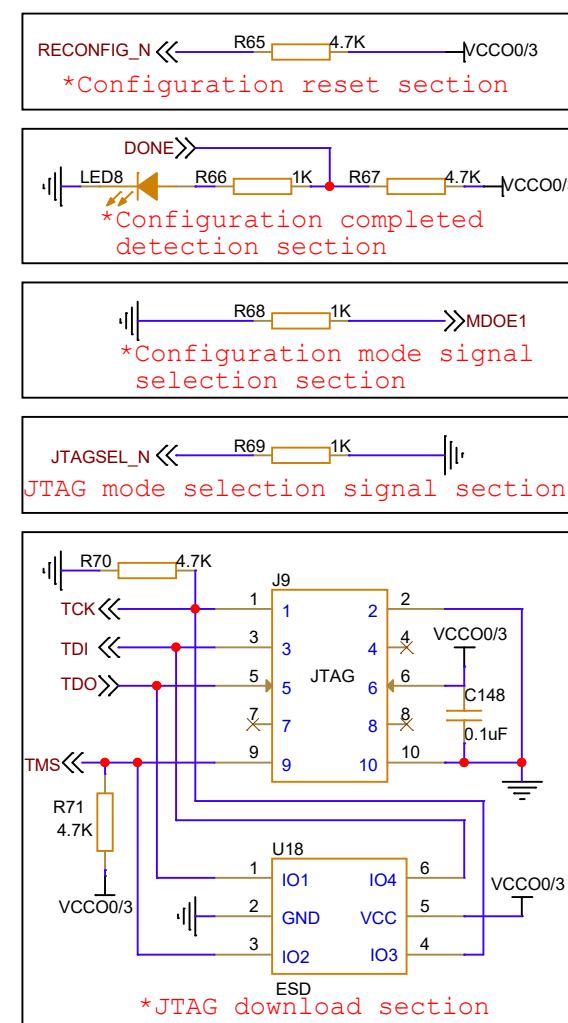
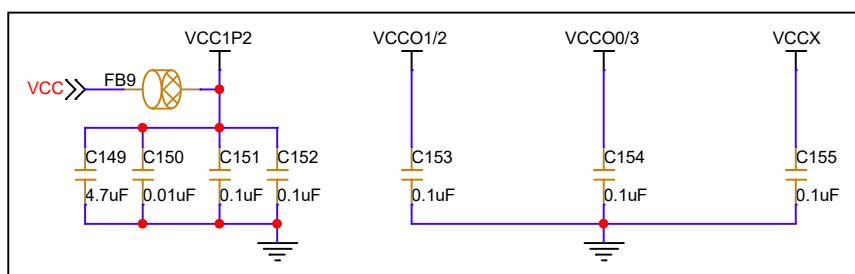
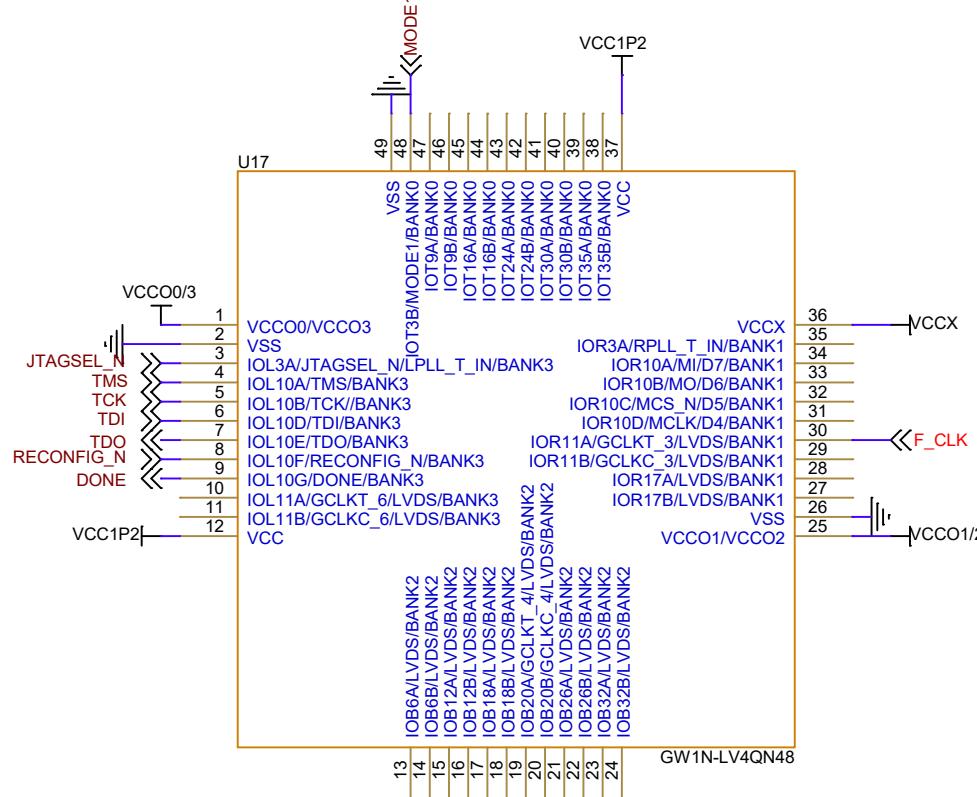
1. $\overline{F_CLK}$ signal is an external input clock signal.

It is recommended that $\overline{F_CLK}$ signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

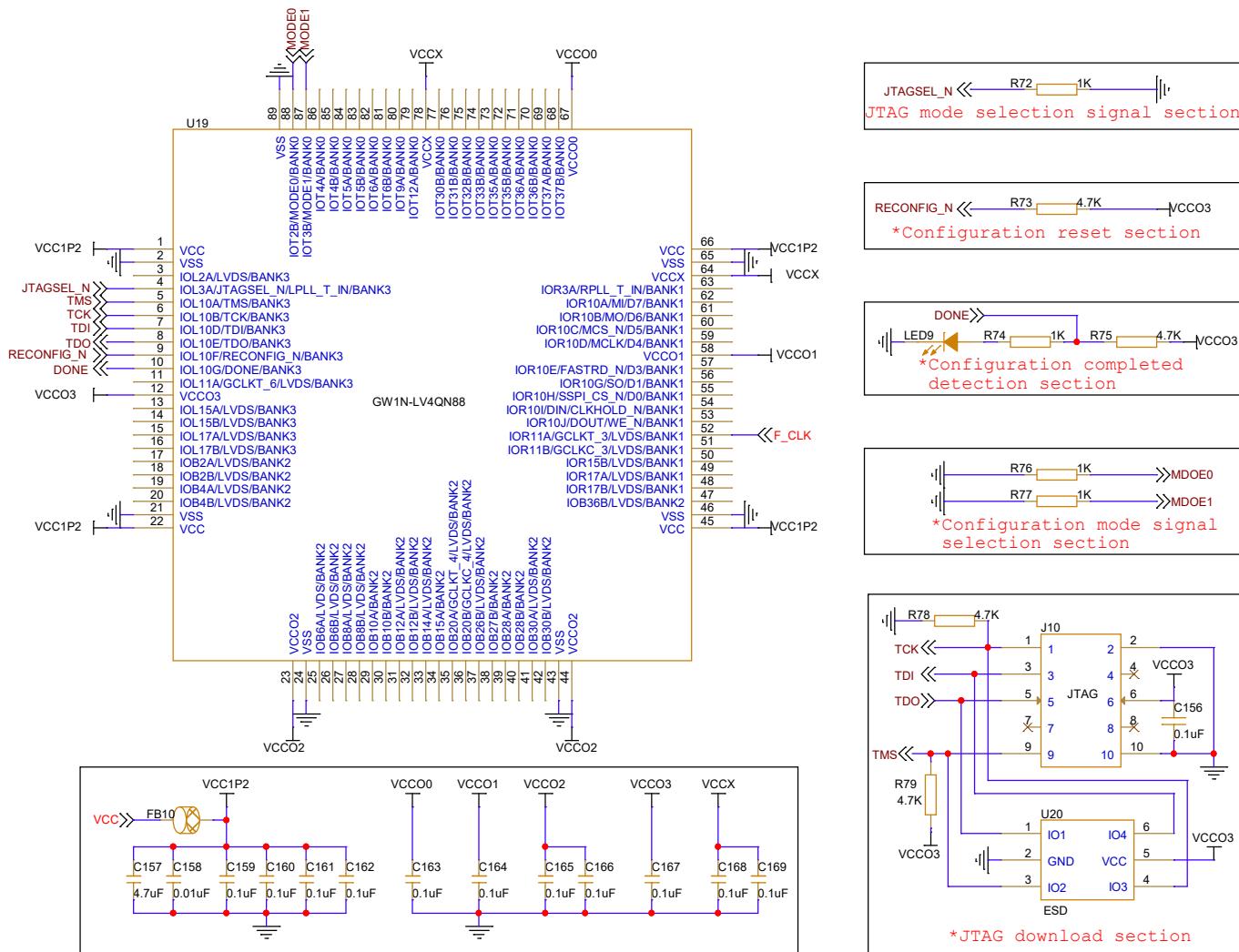
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GOWIN Minimum System Diagram	
Size	Document Number
A4	GW1N-LV4QN32

GW1N-LV4QN48



1. F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

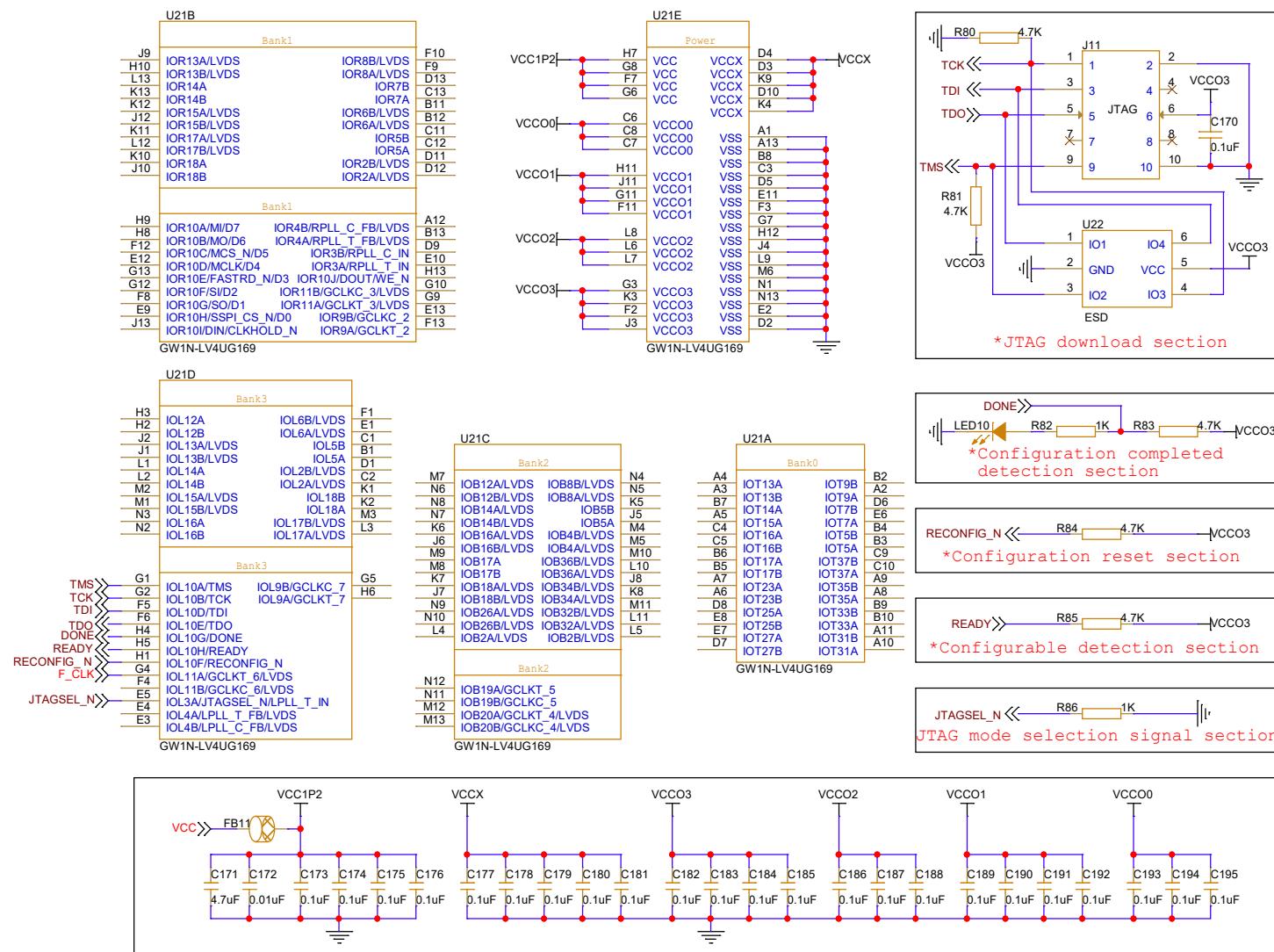
Title	
GOWIN Minimum System Diagram	
Size A4	Document Number GW1N-LV4QN48
Rev 2.1	
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**Notes:**

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size B	Document Number GW1N-LV4QN88
	Rev 2.1

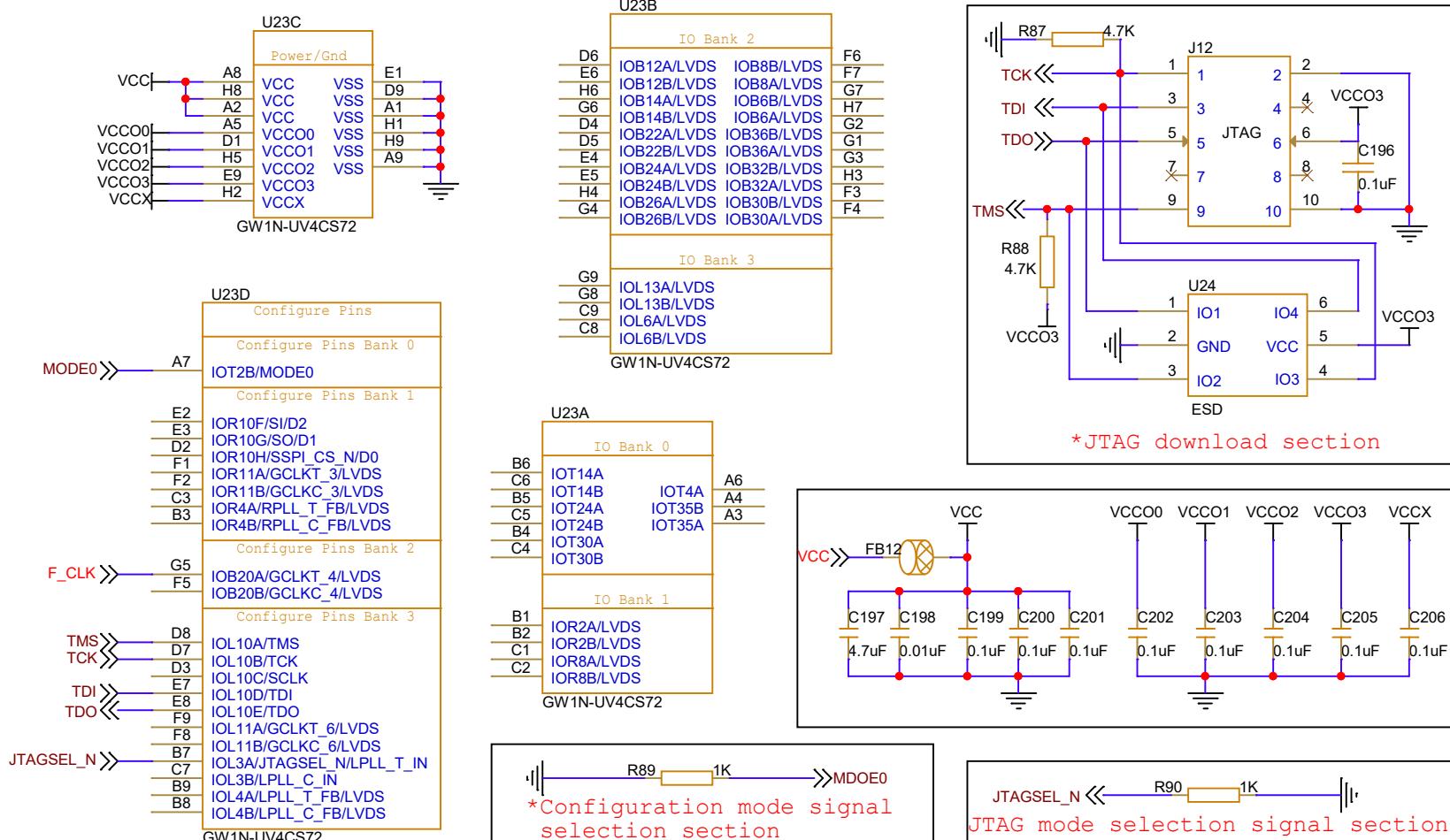
Date: Tuesday, April 09, 2024 Sheet 10 of 22

**Notes:**

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size B	Document Number GW1N-LV4UG169
Rev 2.1	Date: Tuesday, April 09, 2024

GW1N-UV4CS72



Notes:

1. F_CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

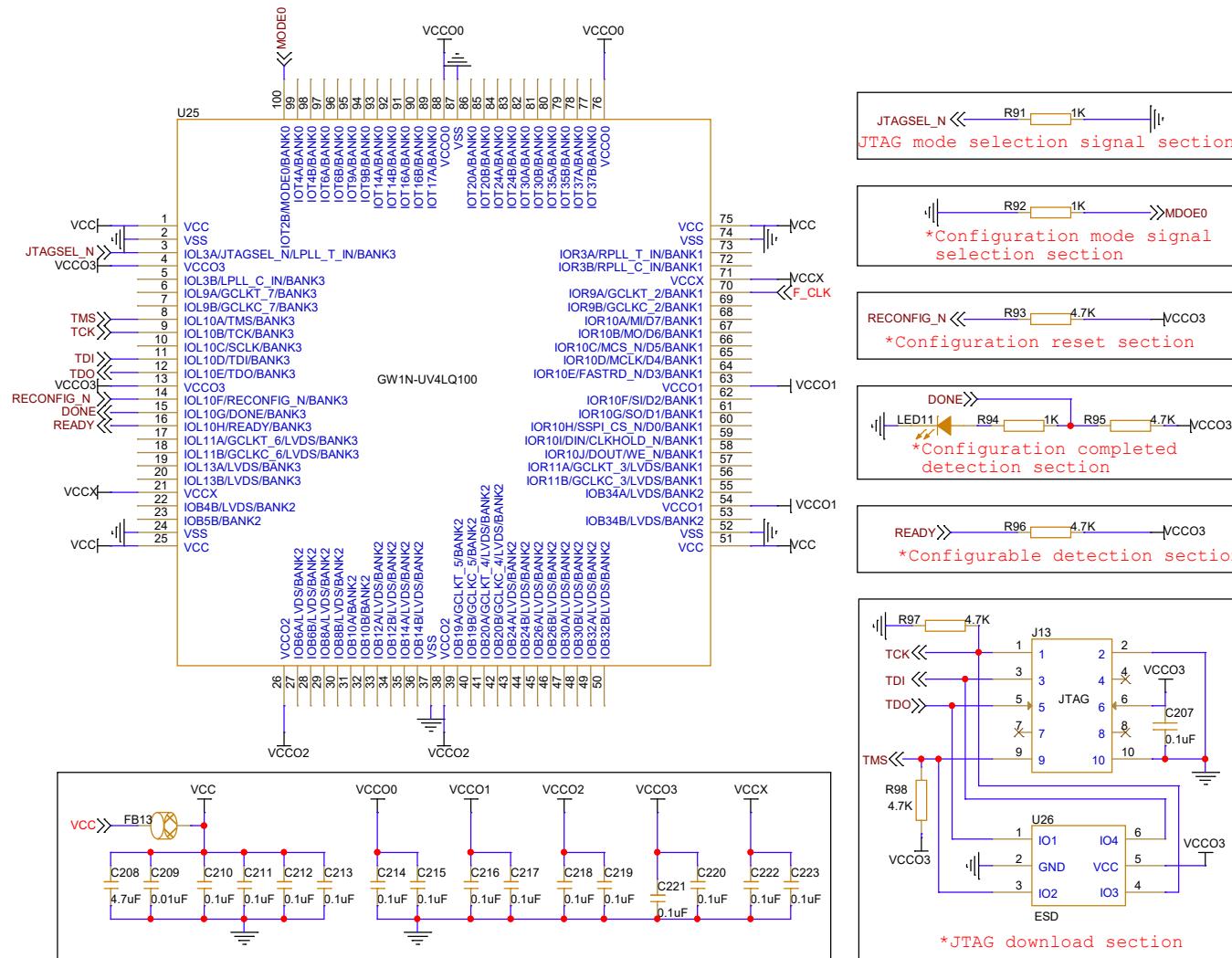
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Size: A4 Document Number: GW1N-UV4CS72

Rev: 2.1

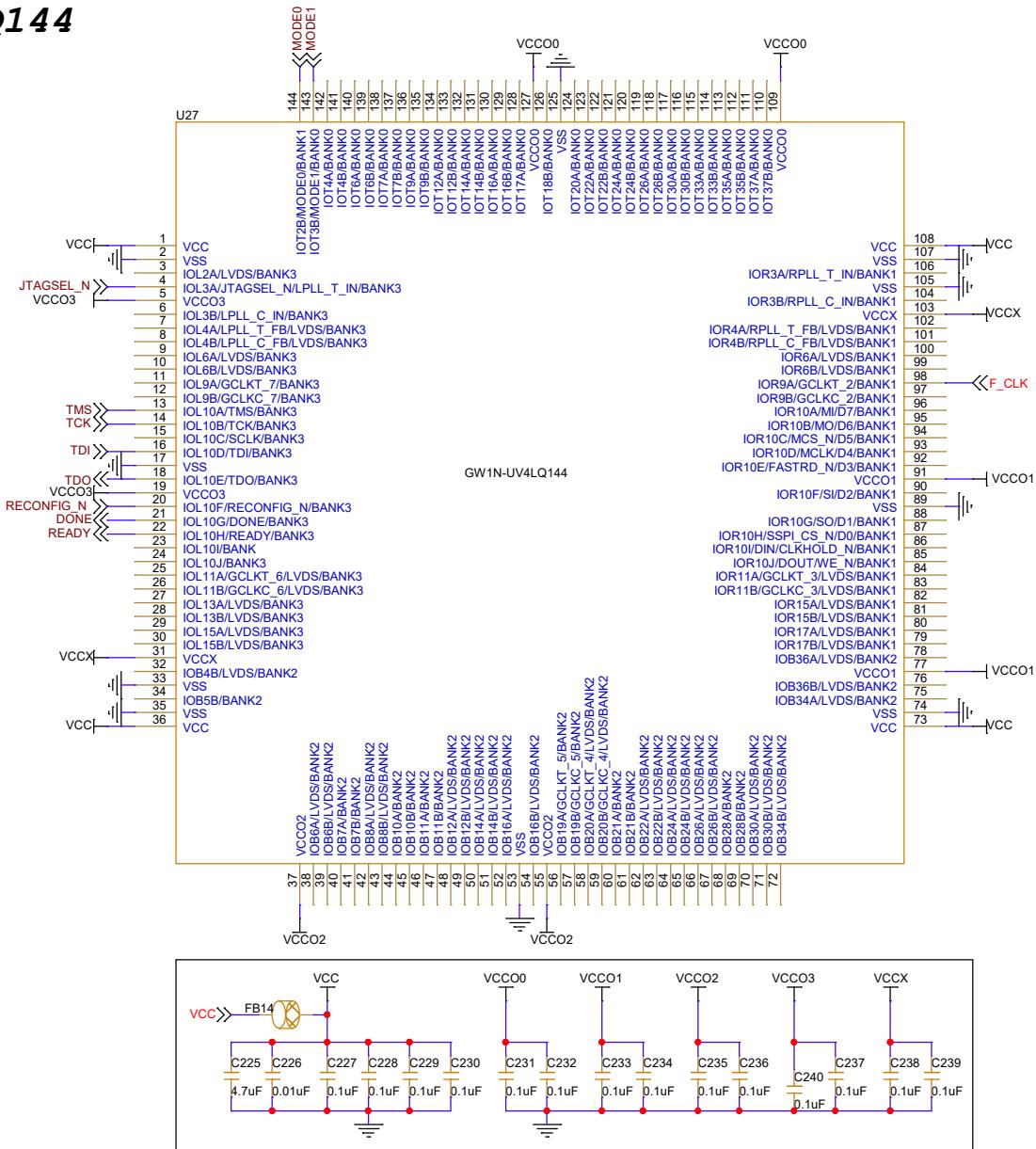
Date: Tuesday, April 09, 2024

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**Notes:**

1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size	Document Number GW1N-UV4LQ100
B	Rev 2.1

**Notes:**

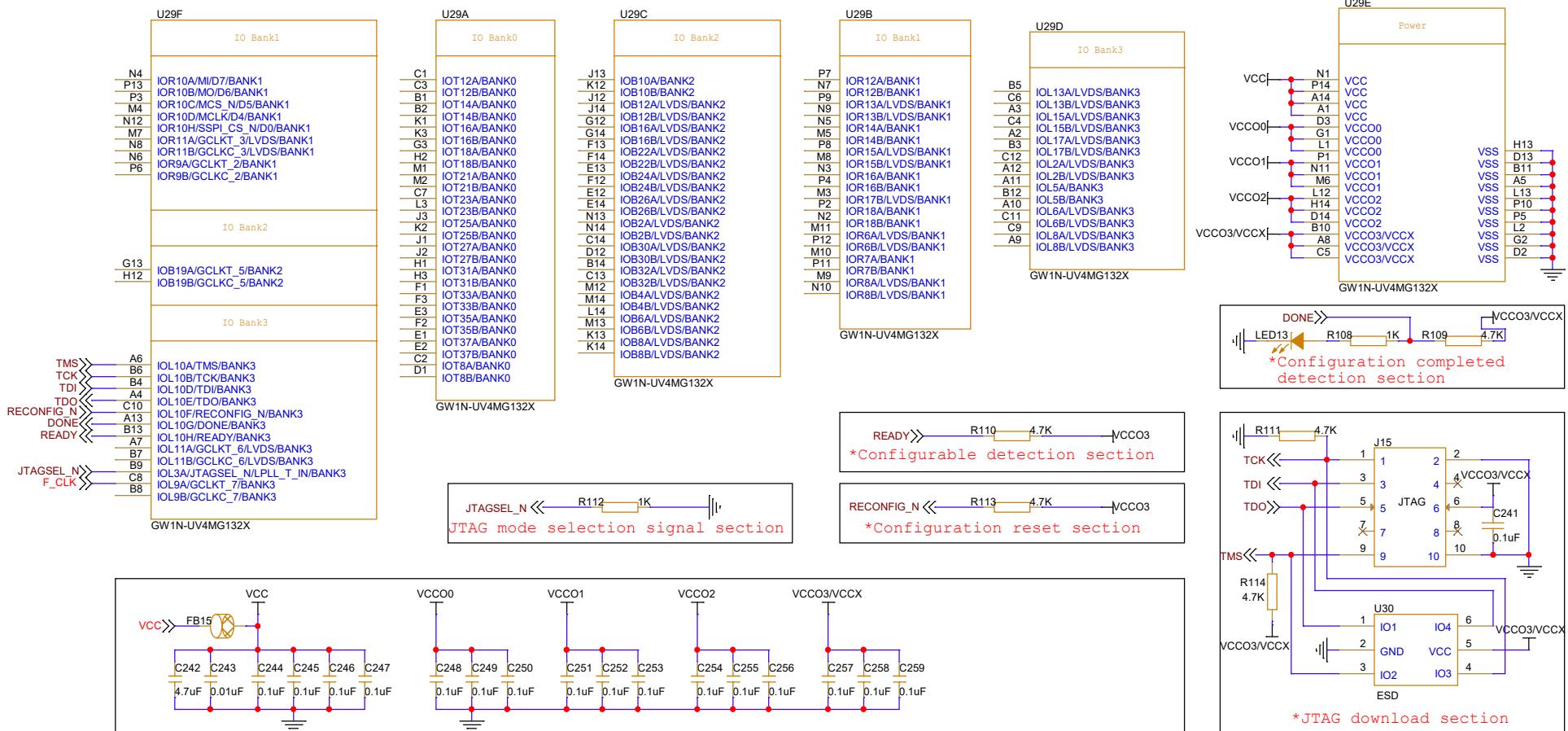
1. F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title: GOWIN Minimum System Diagram

Size: B Document Number: GW1N-UV4LQ144

Rev: 2.1

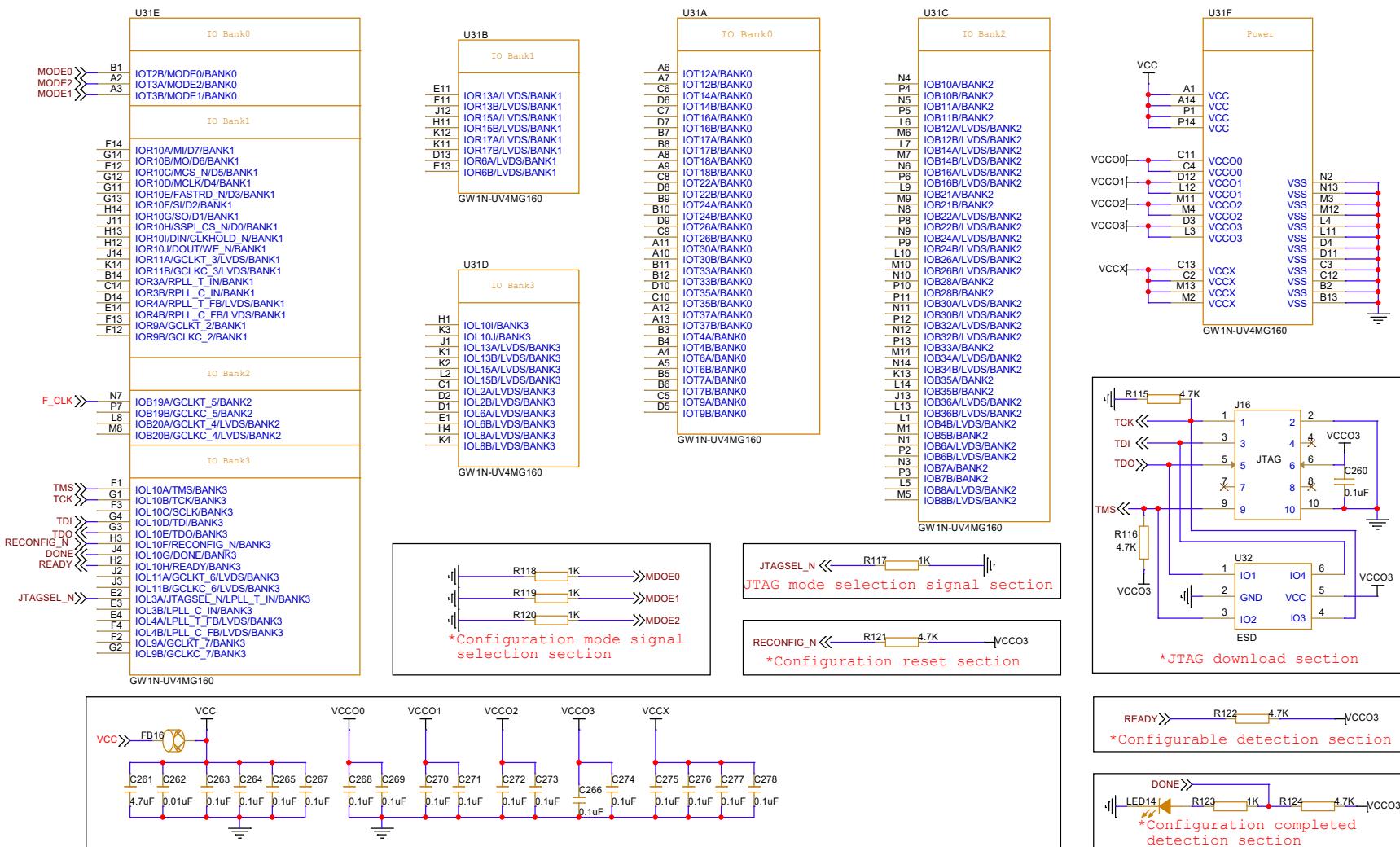
GW1N-UV4MG132X



Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

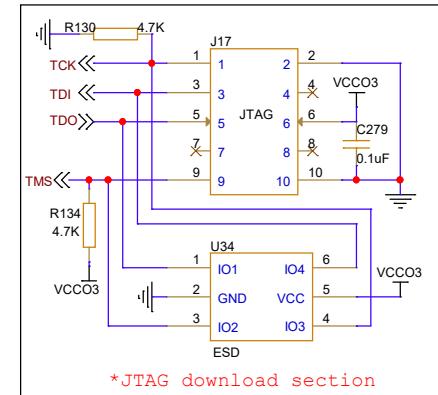
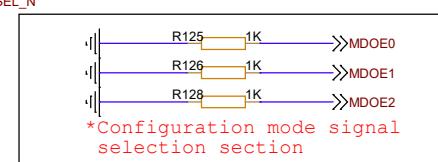
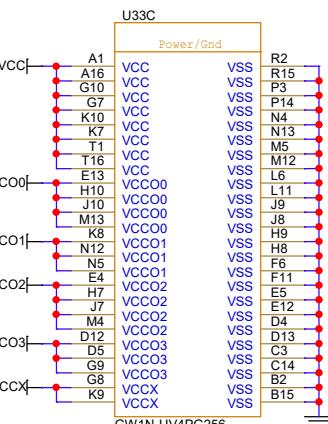
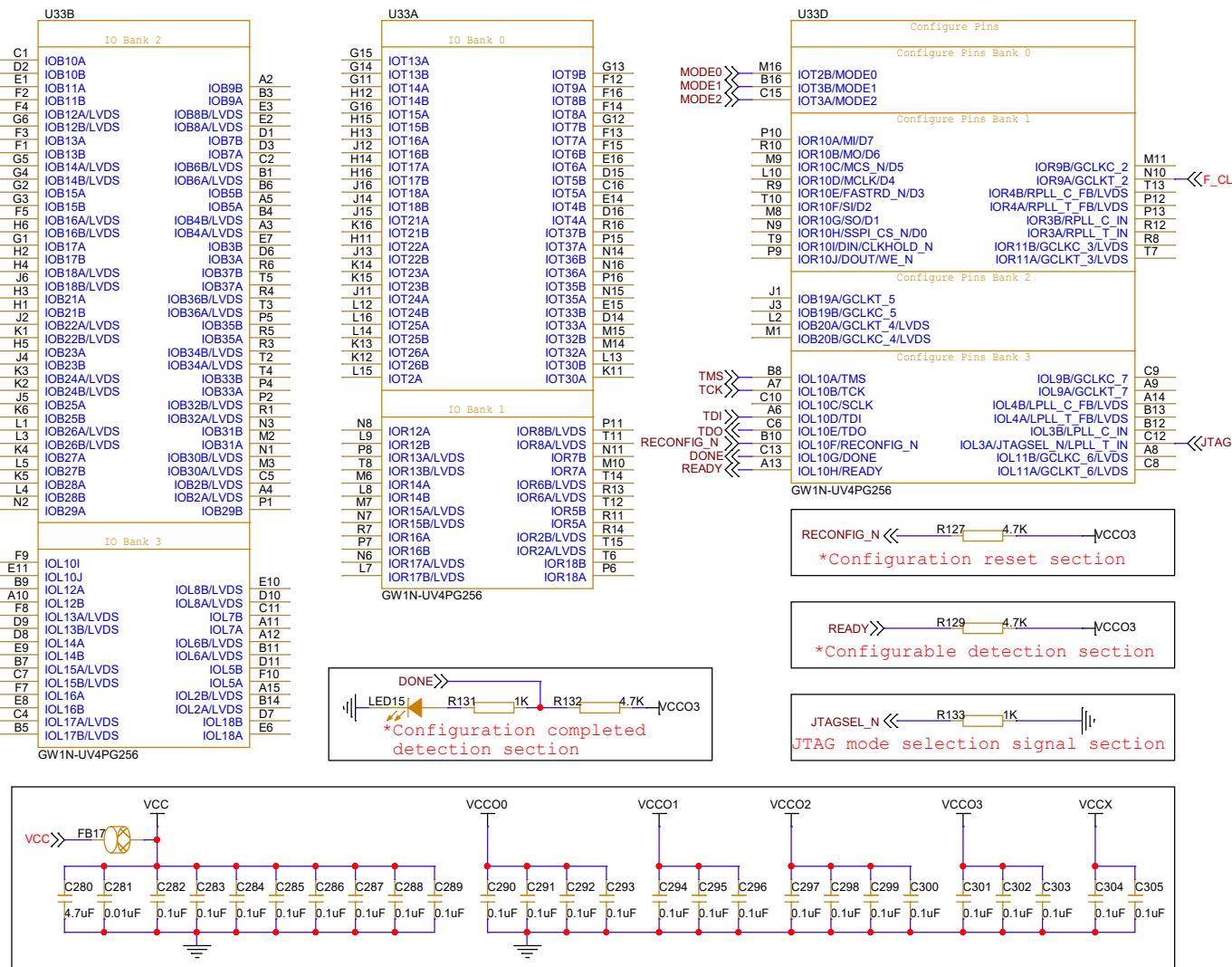
Title		GOWIN Minimum System Diagram		
Size B	Document Number GW1N-UV4MG132X			Rev 2.1
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Notes:

1. F_CLK signal is an external input clock signal.
- It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

GW1N-UV4PG256

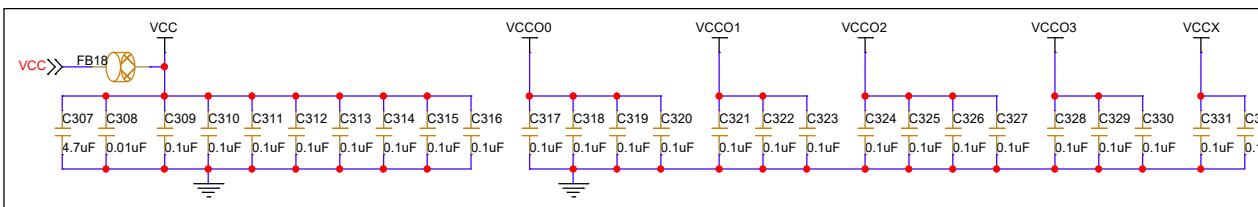
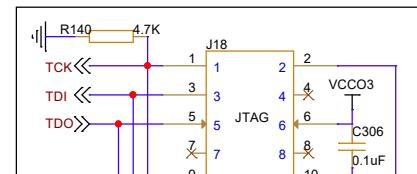
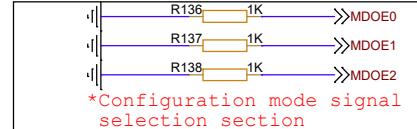
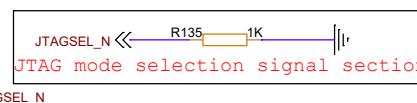
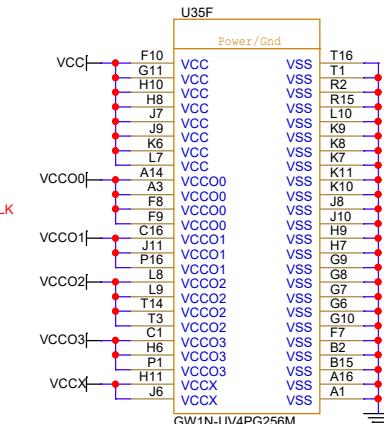
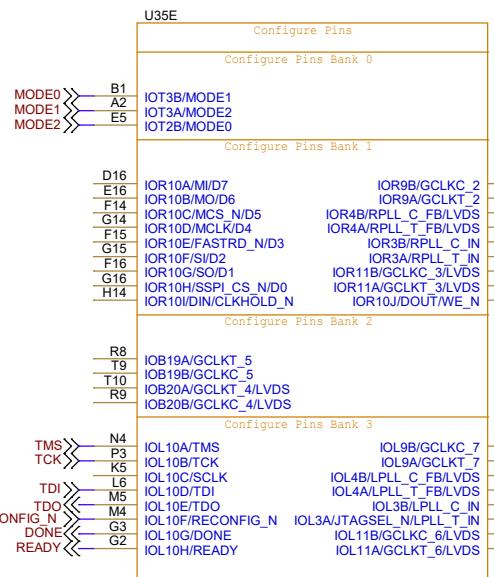
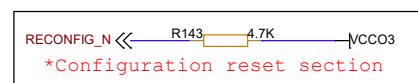
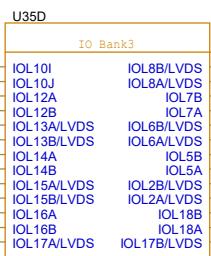
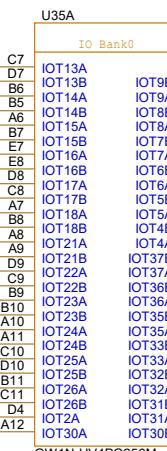
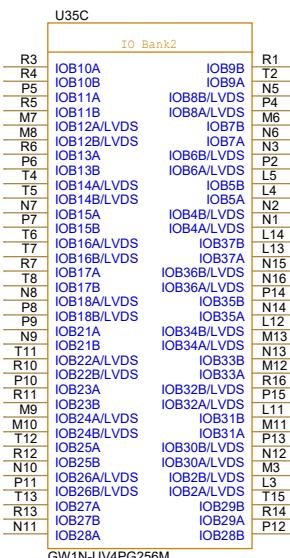


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		GOWIN Minimum System Diagram		
Size		Document Number		
B		GW1N-UV4PG256		Rev 2.1
Date:	Tuesday, April 09, 2024	Sheet	17	of 22

GW1N-UV4PG256M



Notes:

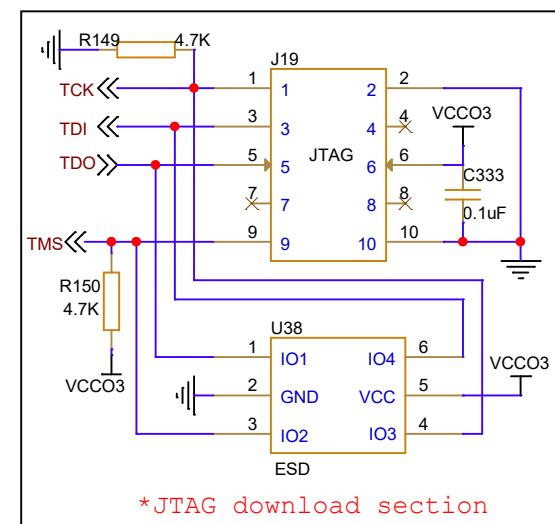
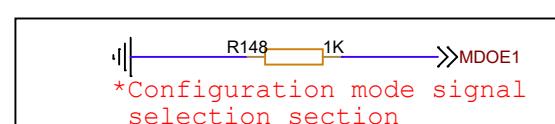
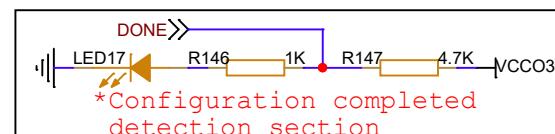
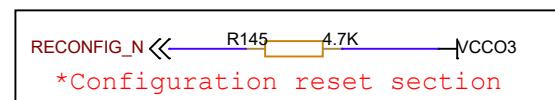
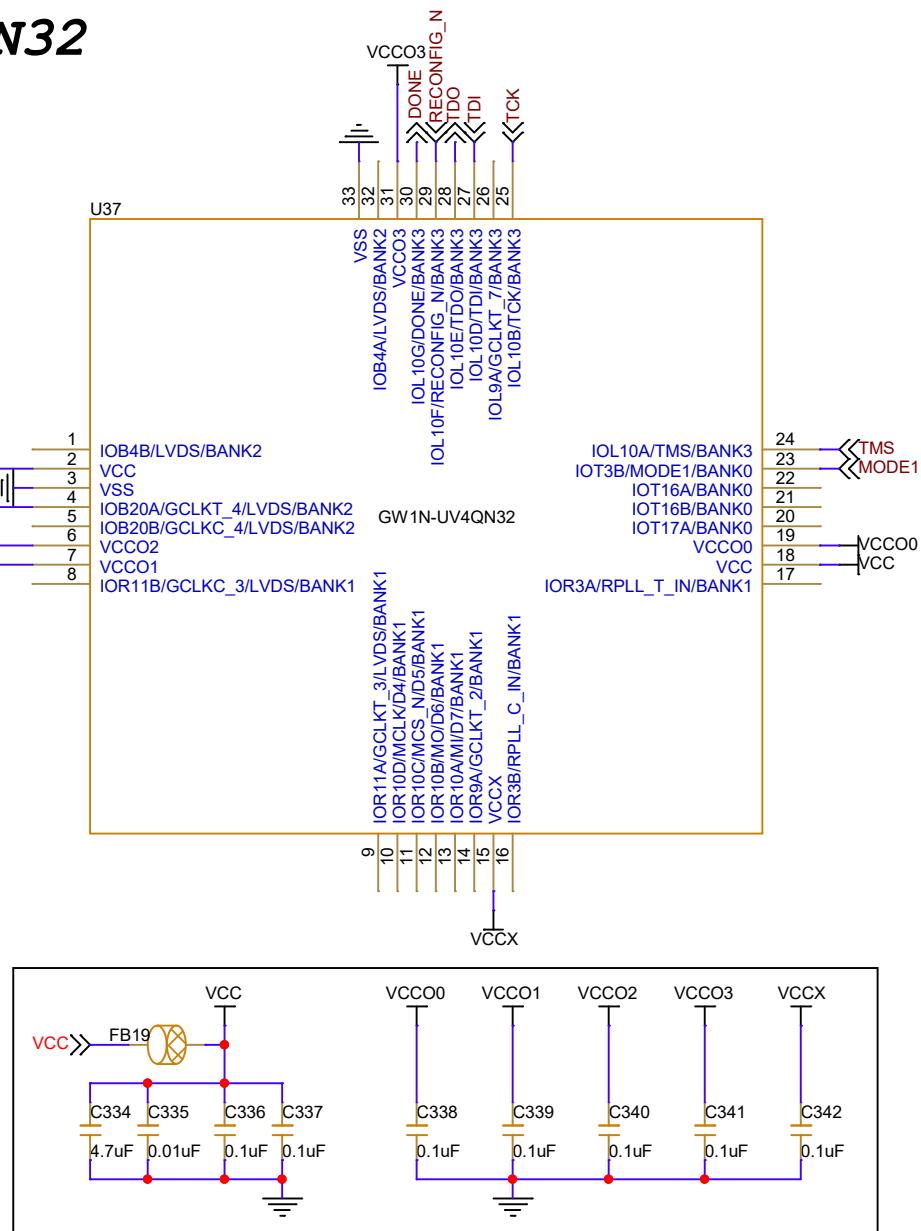
- NOTES:

 - 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number GW1N-UV4PG256M	Rev 2.1
Date: Tuesday, April 09, 2024	Sheet 18	of 22

GW1N-UV4QN32

5 4 3 2 1



Notes:

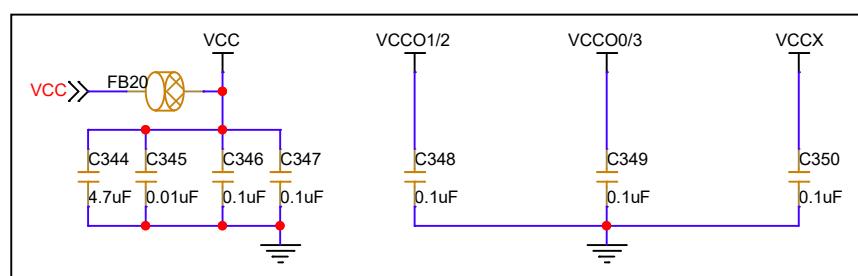
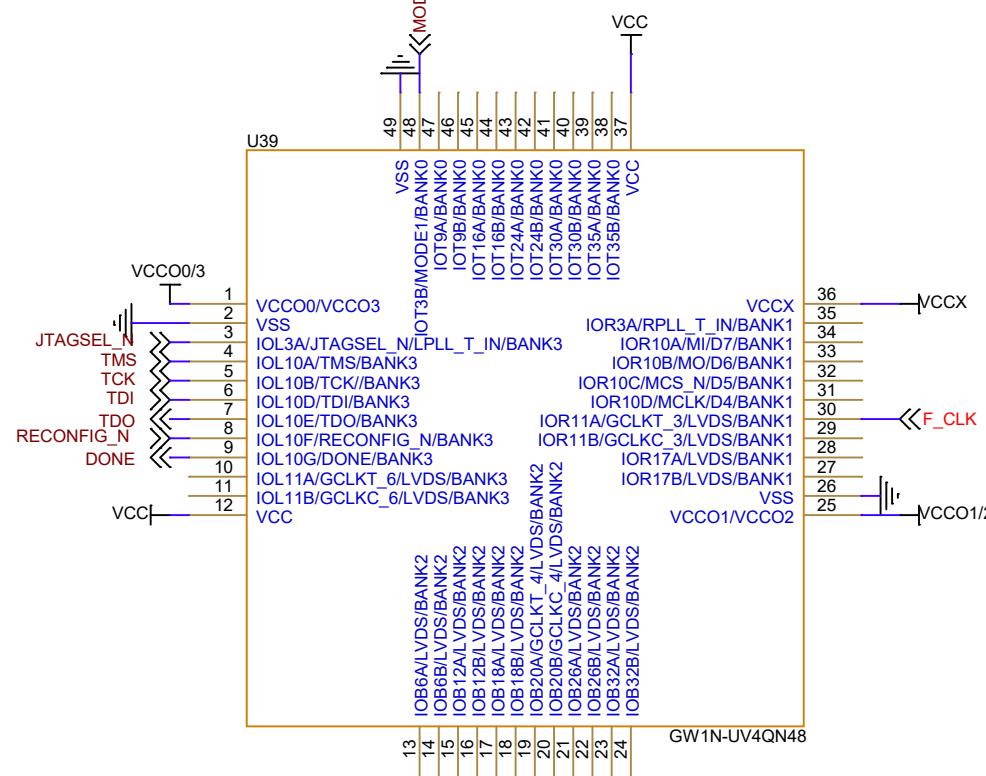
1. F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GWIN Minimum System Diagram	
Size	Document Number
A4	GW1N-UV4QN32
Date:	Tuesday, April 09, 2024
Rev	2.1

GW1N-UV4QN48

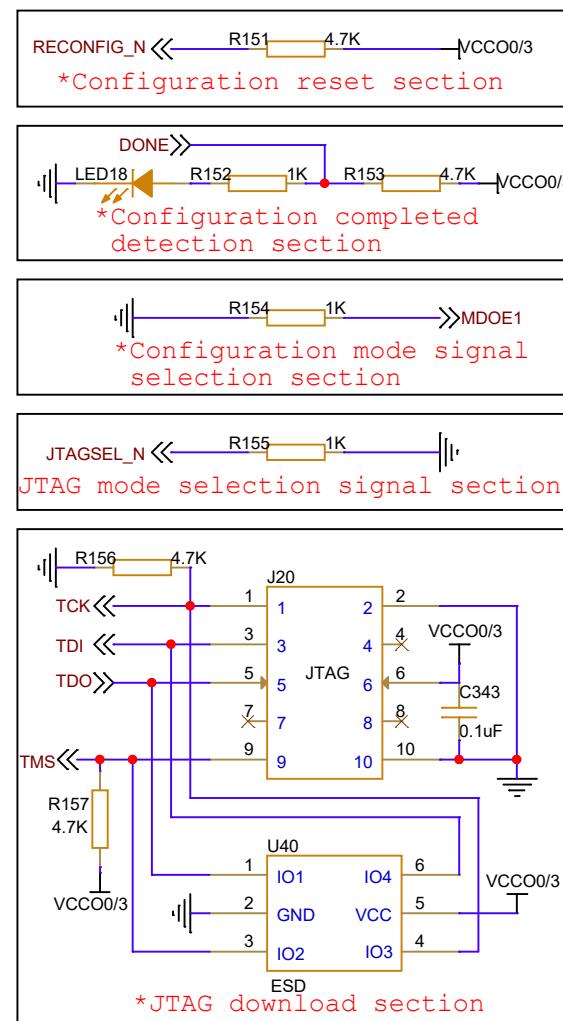


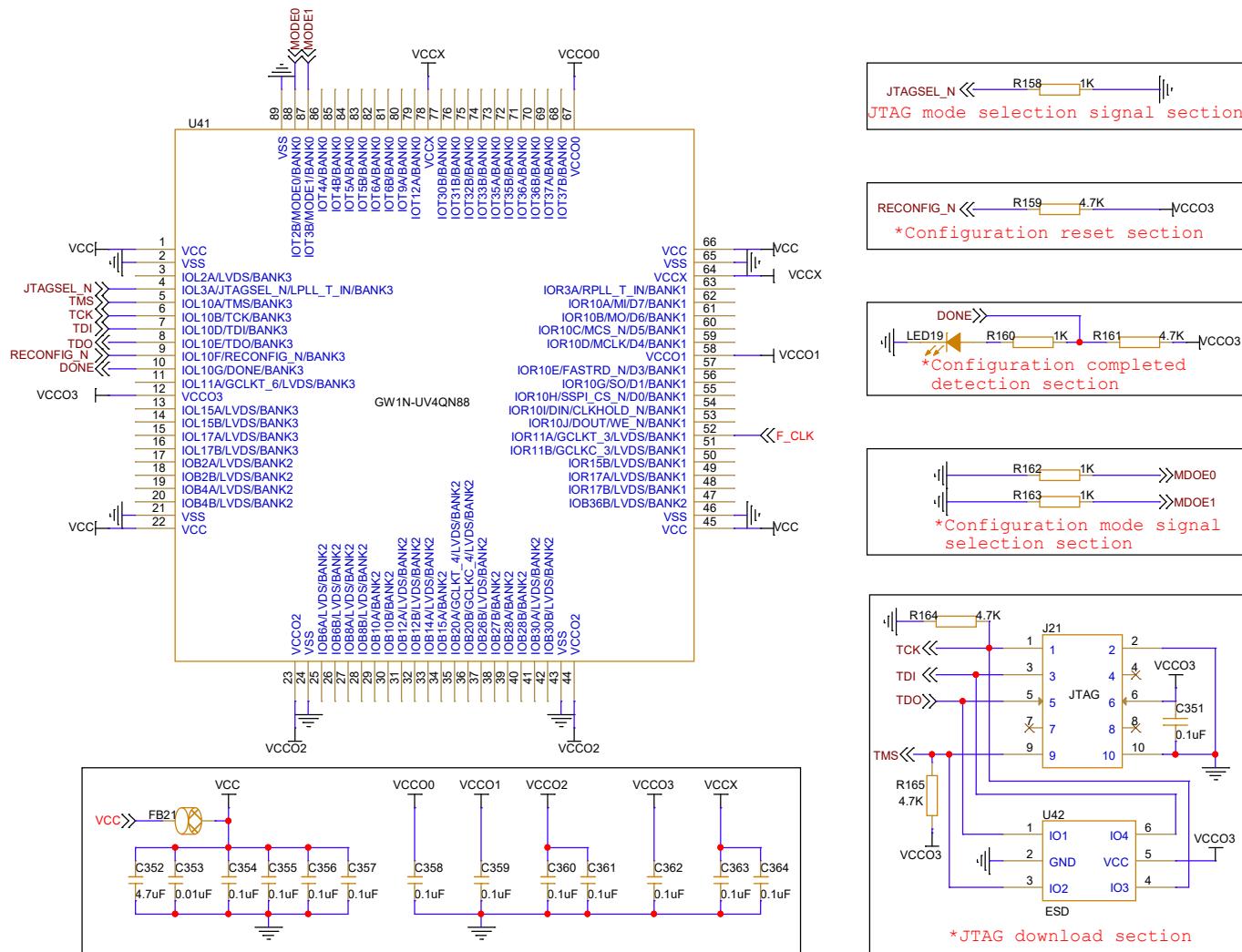
Notes:

1. F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.





Notes:

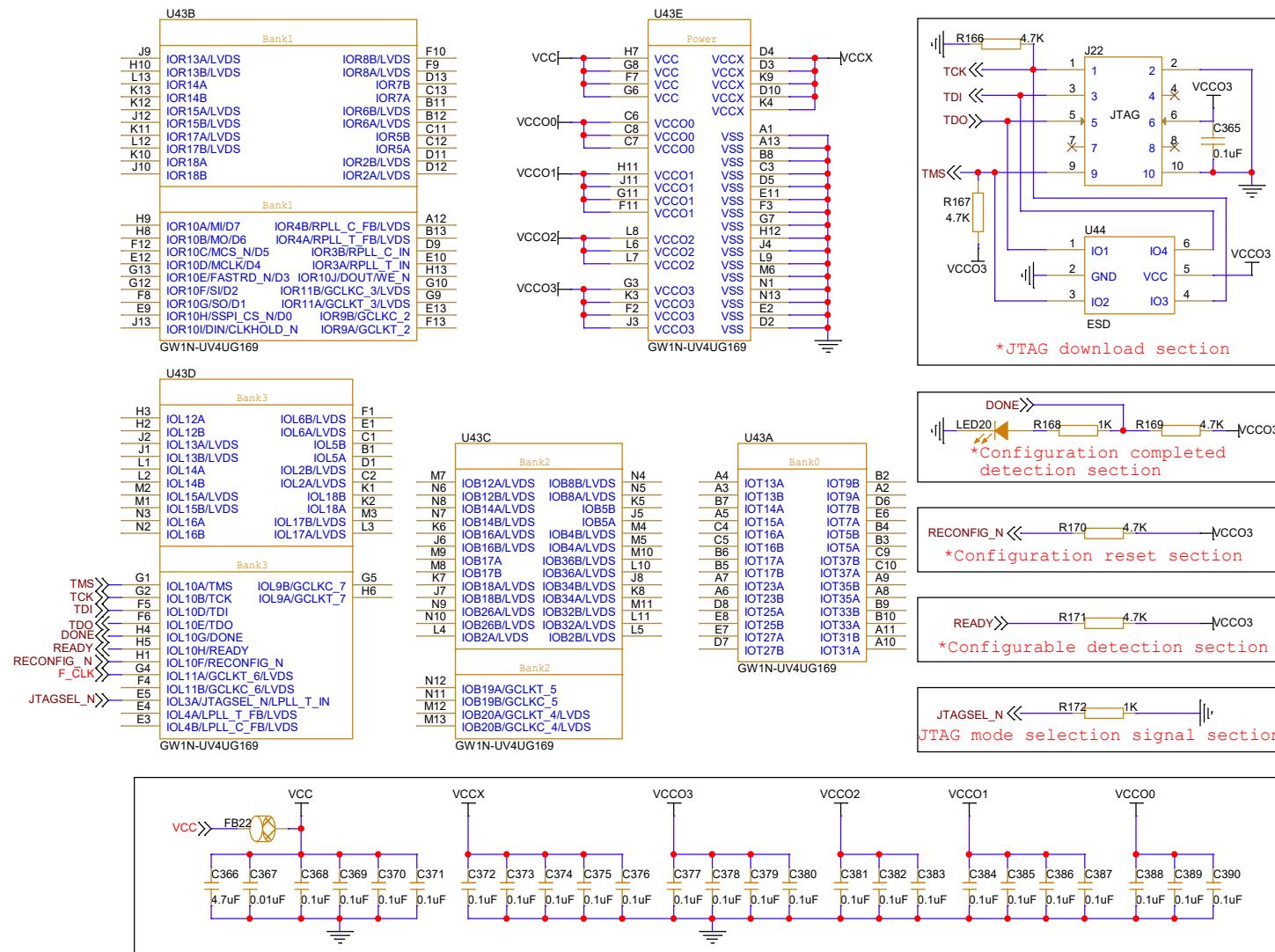
1. F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title	
GOWIN Minimum System Diagram	
Size	Document Number
B	GW1N-UV4QN88
	Rev 2.1
Date: Tuesday, April 09, 2024	Sheet 21 of 22

GW1N-UV4UG169



Notes

- Notes:

 - 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number GW1N-UV4UG169	Rev 2.1
Date Tuesday, April 29, 2024	Sheet 23	of 23