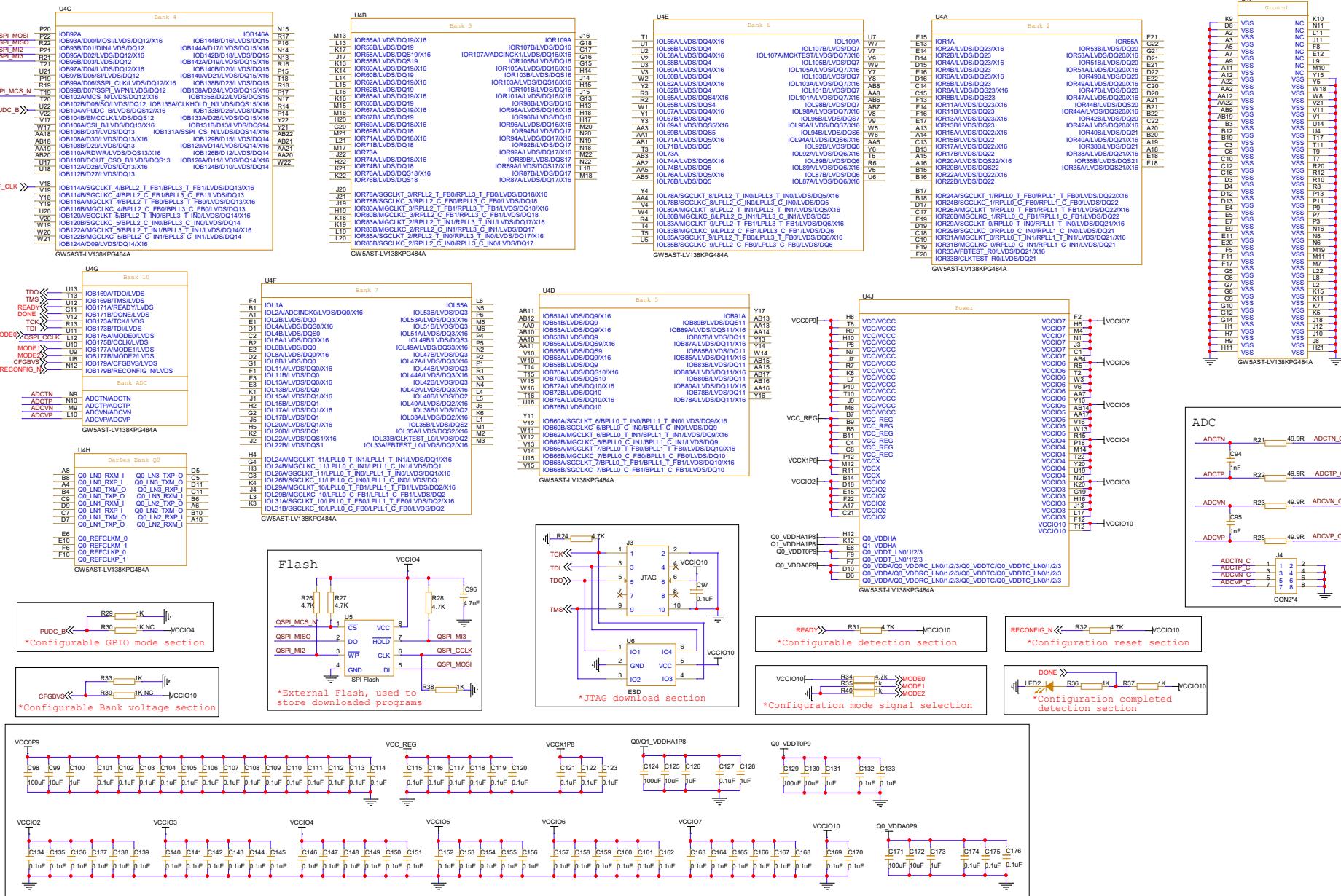


Notes:

- FCLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- External Flash memory is used to store downloaded programs.
- For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704, Arora V FPGA Products Programming and Configuration Guide .
- It is recommended that add an ESD protection chip to the JTAG download circuit.
- VCC core voltage requires a large current, so it is recommended to supply power separately.
- The MODE pin is the GowinCONFIG configuration mode selection signal.
- For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG704, Arora V FPGA Products Programming and Configuration Guide .



Notes:
1. E-GW is a local indicator of the degree of localisation.

1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator/crystal.

it is recommended that FCLK signal be provided through an active External Flash memory is used to store downloaded programs.

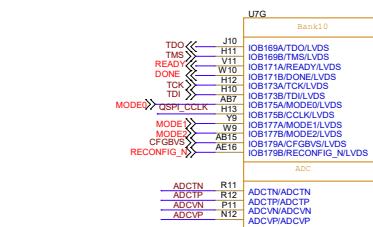
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection".

For details about specific model selection, see Chapter 11 of the **Aurora V FPGA Products Programming and Configuration Guide**.

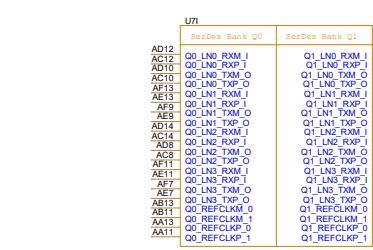
3. It is recommended that add an ESD protection chip to the JTAG download circuit.
4. VCC core voltage requires a large current, so it is recommended to supply power separately.

Title		GOWIN Minimum System Diagram		
Size		Document Number		Rev.
A2		GW5AST-LV138P4G4A		2.1
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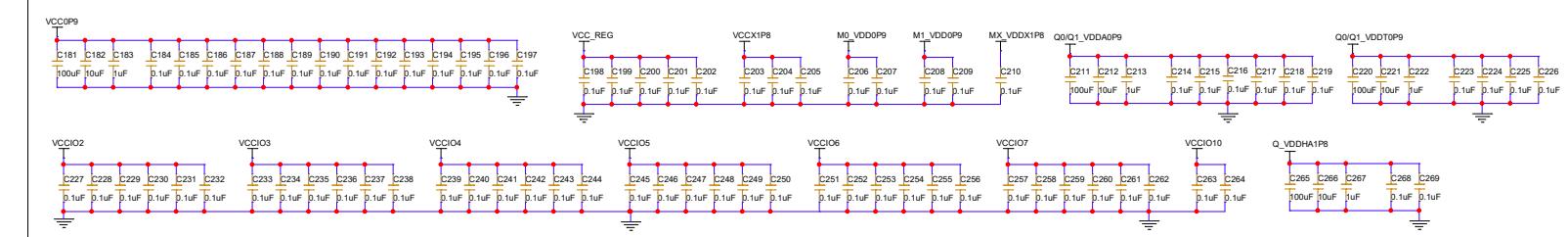
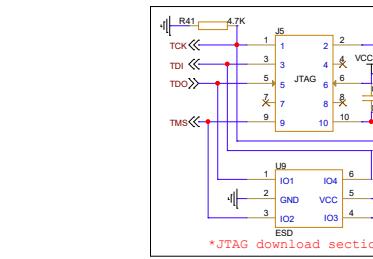
GW5AST-LV138PG676A



GW5AST-138K-PG676A



GW5AST-138K-PG676A



Notes:

Notes:
1.F CLK signal is an external input clock signal.

It is recommended that F CLK signal be provided through an active driver.

2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG704,

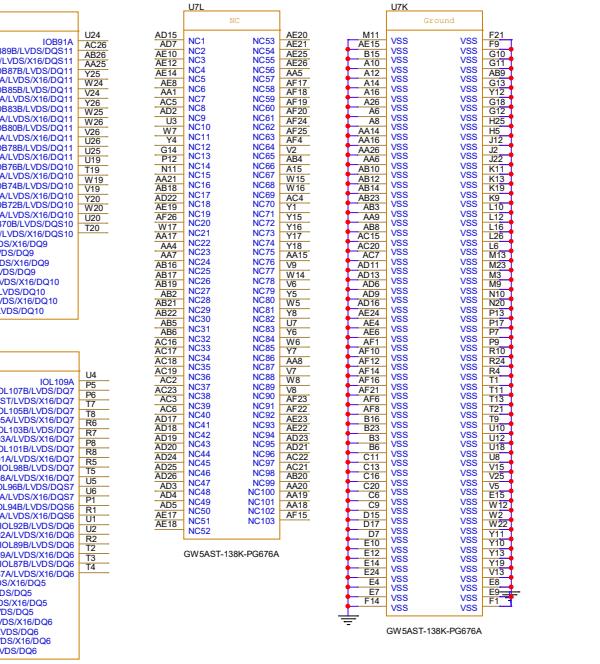
Arora V FPGA Products Programming and Configuration Guide .

3. It is recommended that add an ESD protection chip to the JTAG download circuit.

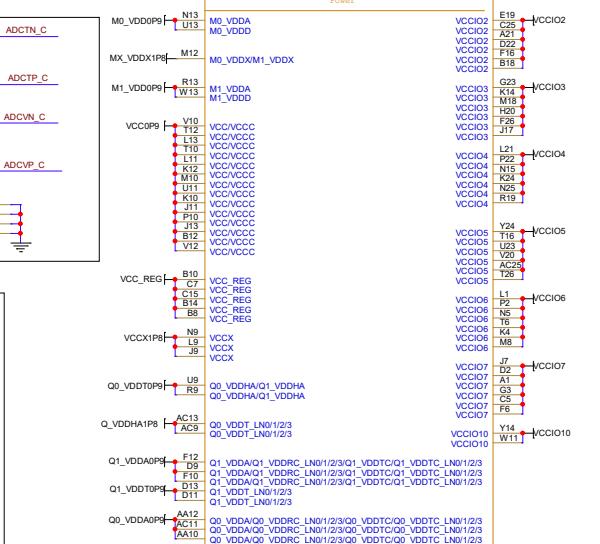
4. VCC core voltage requires a large current, so it is recommended to

5. The MODE pin is the GowinCONFIG configuration mode selection signal.

For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in the [Xilinx® FPGA Product Programming and Configuration Guide](#).



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GW5AST-138K

