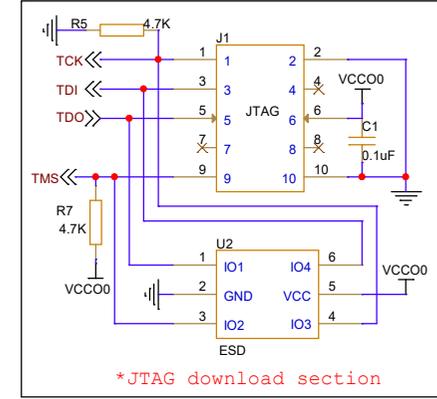
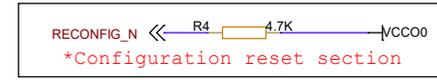
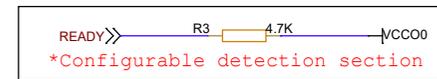
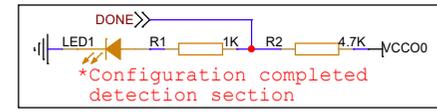
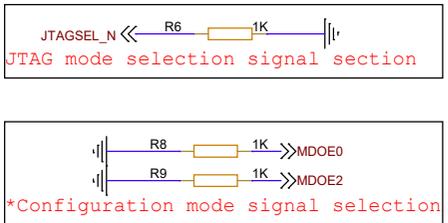
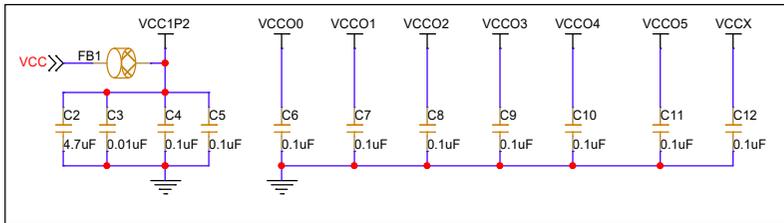
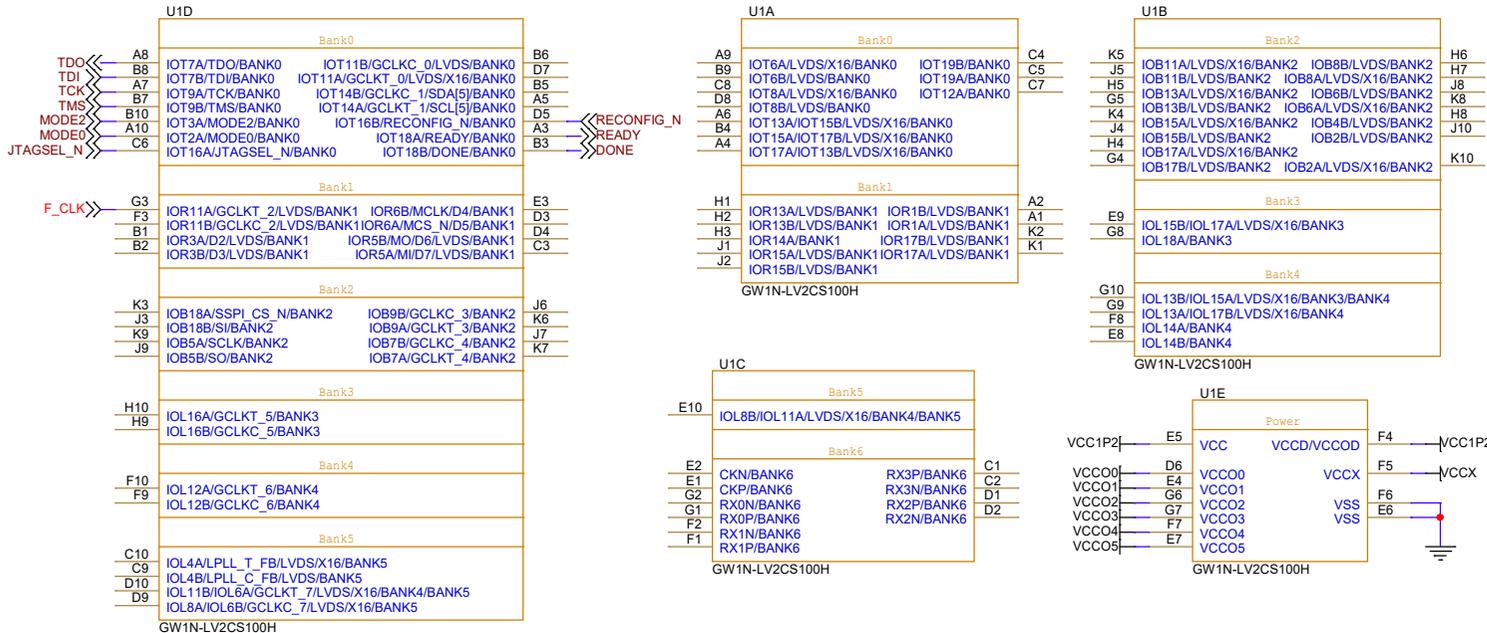


GW1N-LV2CS100H

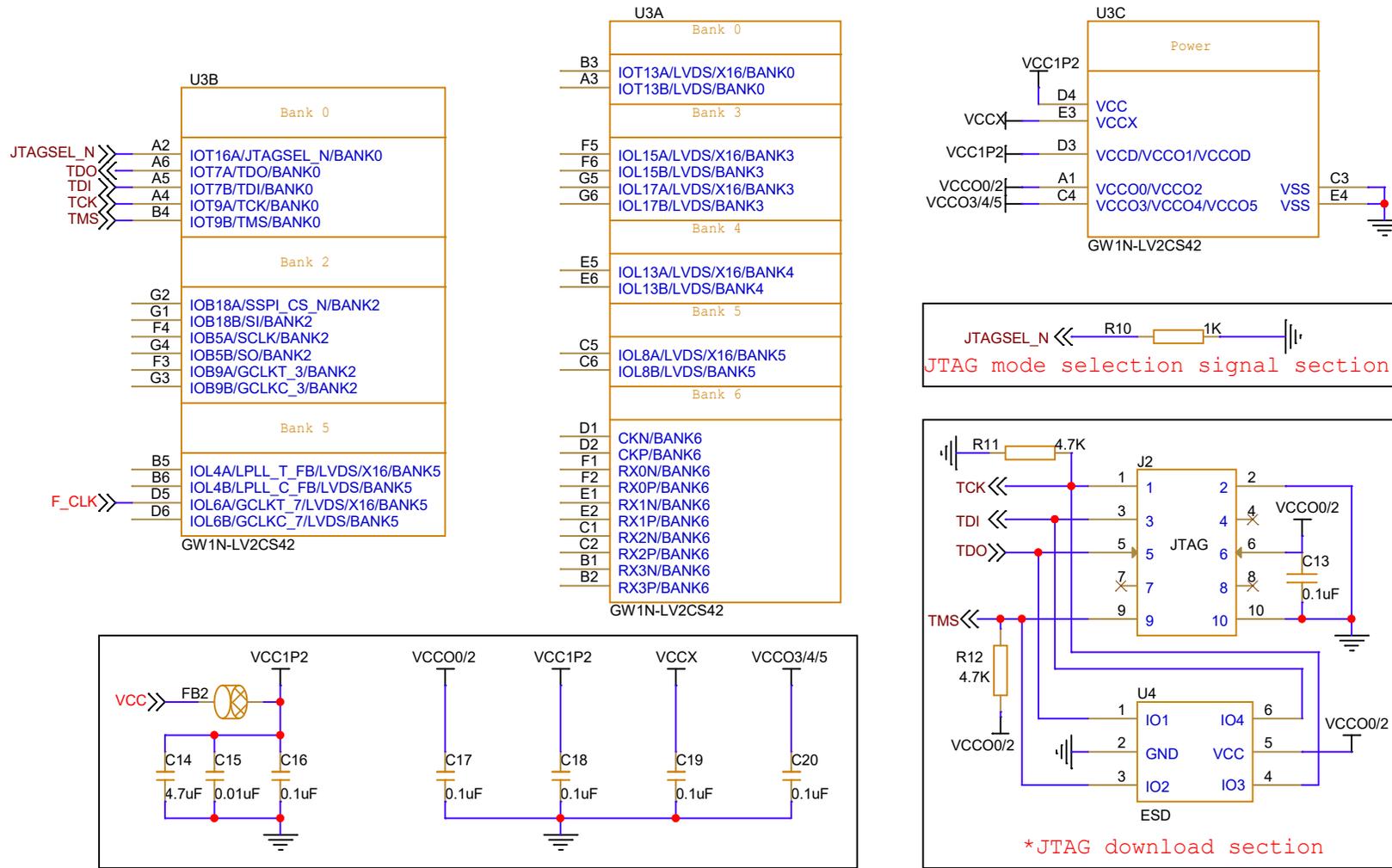


Notes:

- 1.F CLK signal is an external input clock signal.
- It is recommended that F CLK signal be provided through an active oscillator crystal.
- It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number GW1N-LV2CS100H	Rev 2.1
Date: Tuesday, April 09, 2024	Sheet 1 of 33	

GW1N-LV2CS42

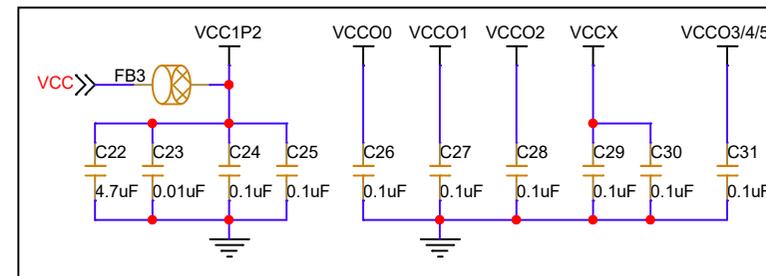
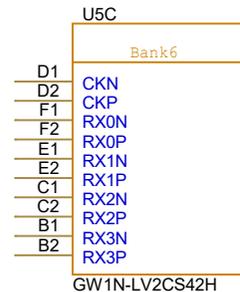
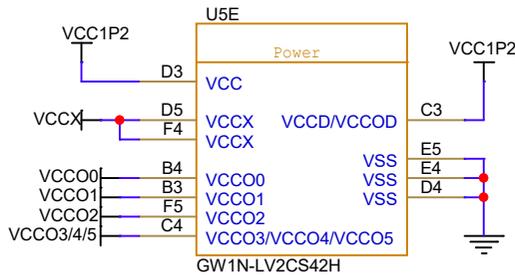
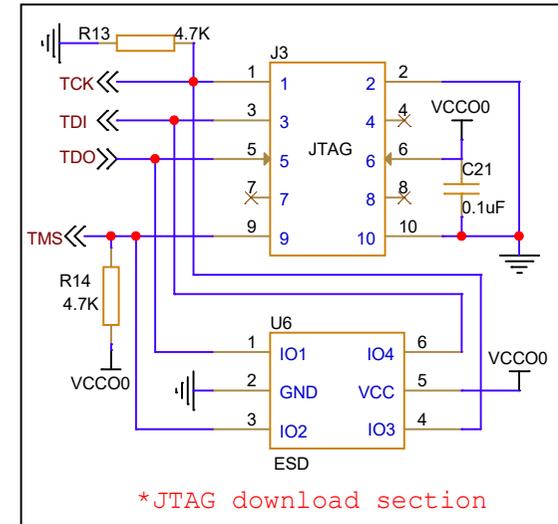
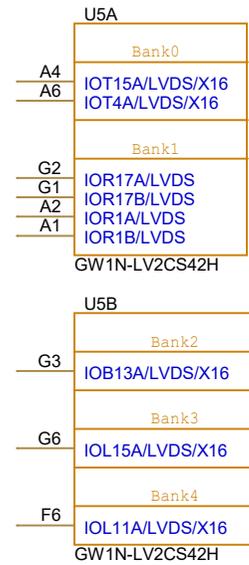
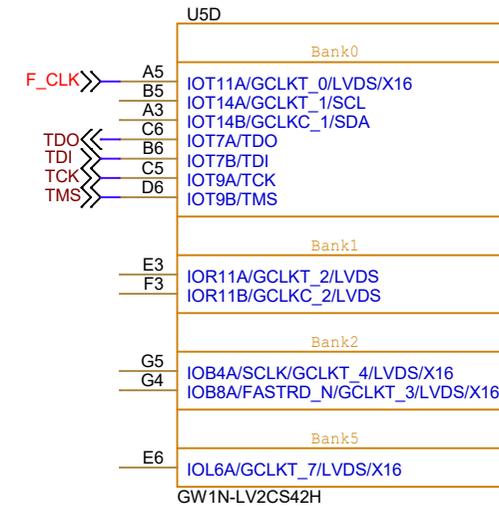


Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1N-LV2CS42	2.1
Date:	Wednesday, April 10, 2024	Sheet 2 of 33

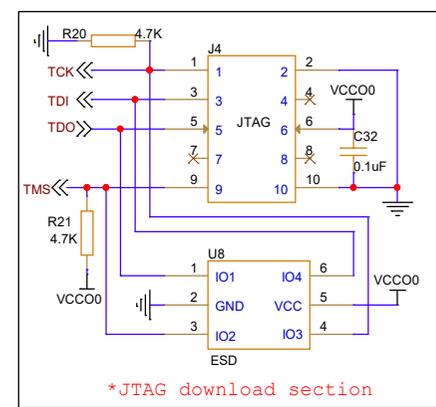
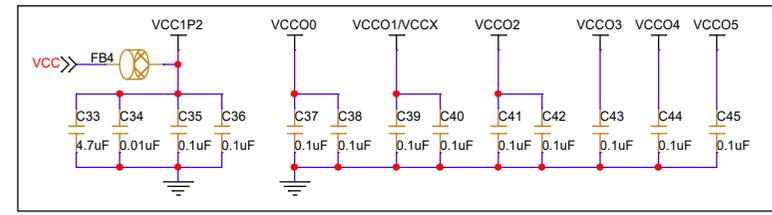
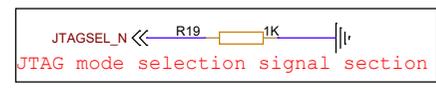
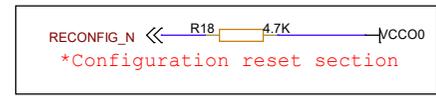
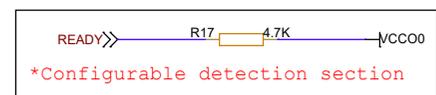
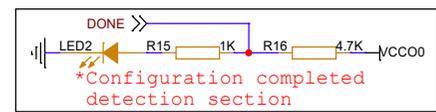
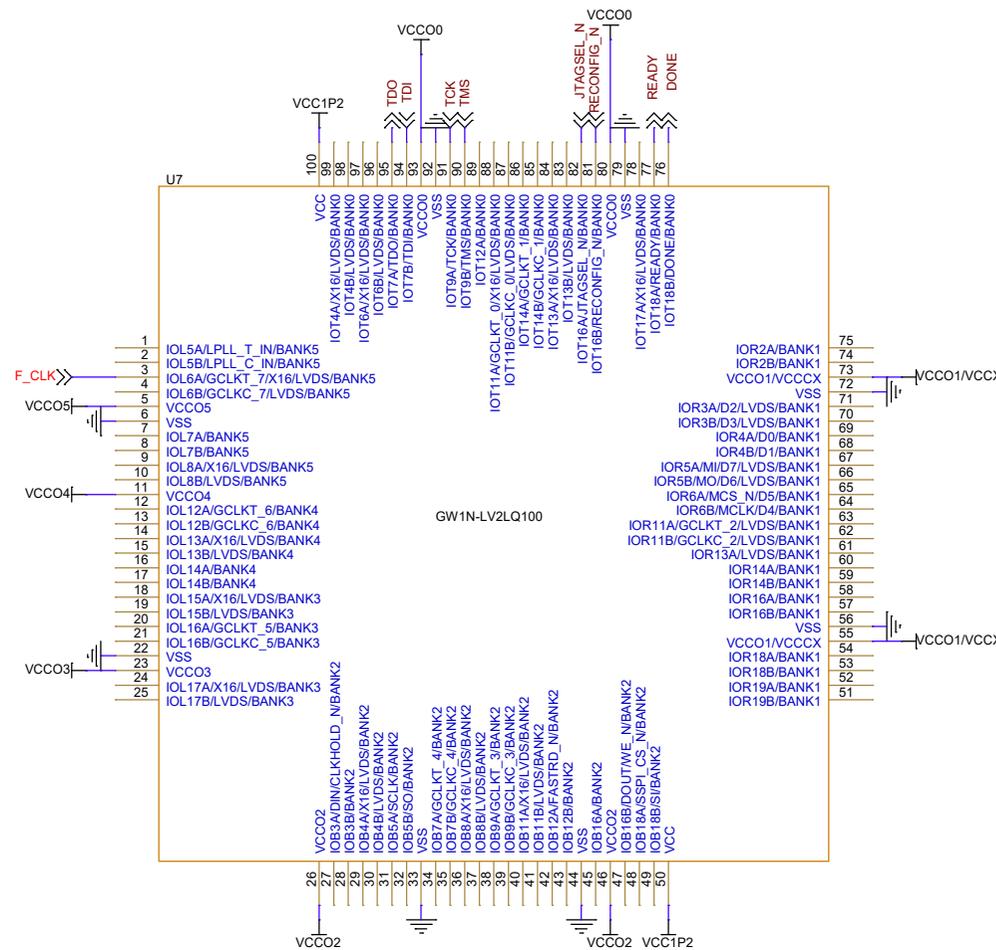
GW1N-LV2CS42H



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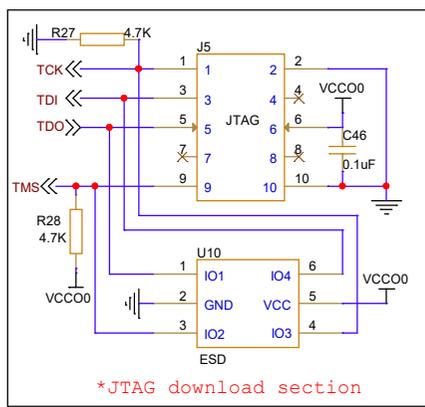
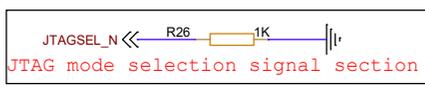
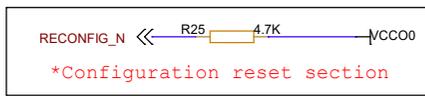
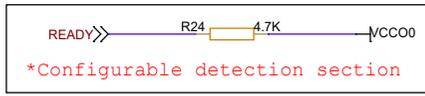
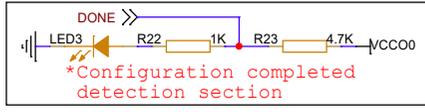
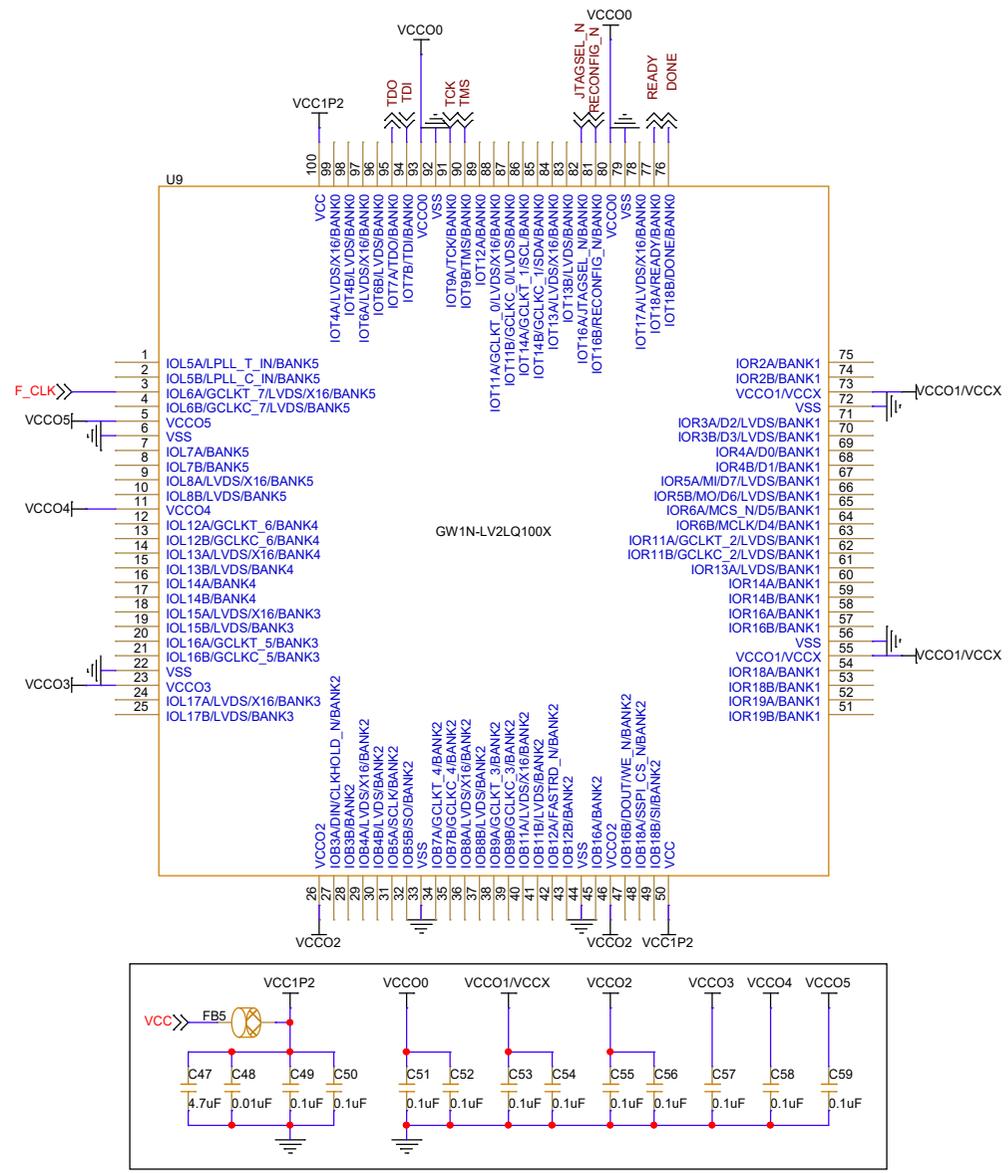
1. F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1N-LV2CS42H	2.1
Date:	Tuesday, April 09, 2024	Sheet 3 of 33



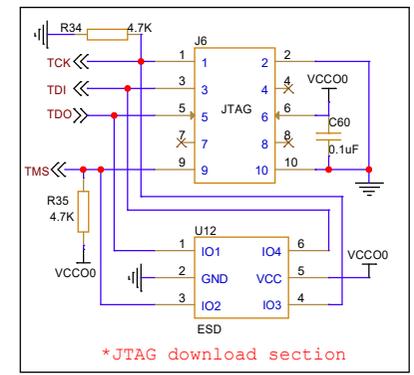
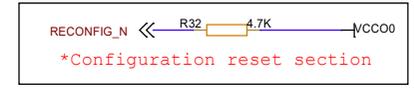
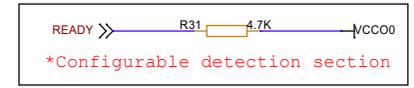
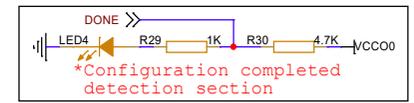
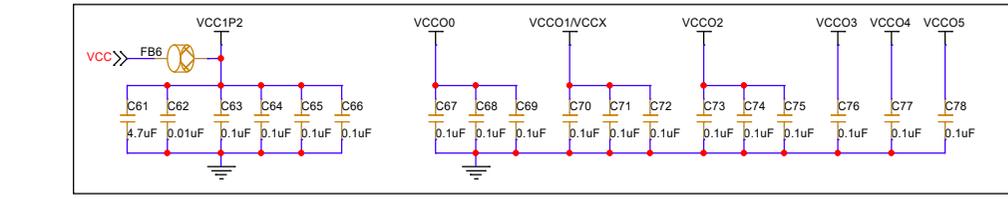
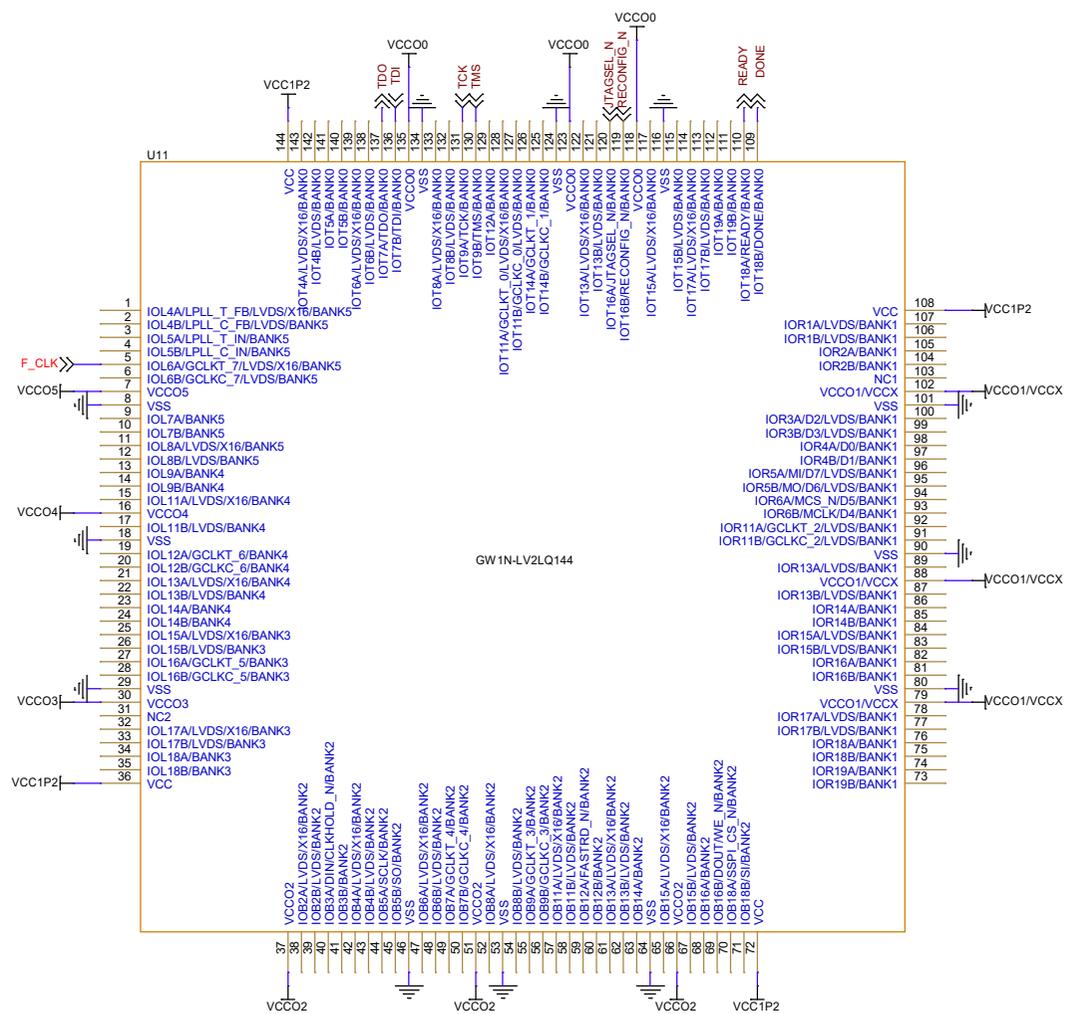
Notes:
 1.F CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
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Date:	Tuesday, April 09, 2024	Sheet 4 of 33

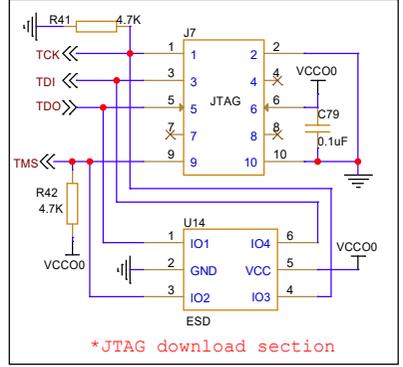
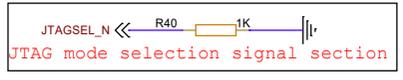
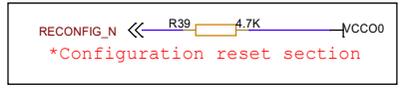
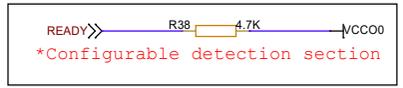
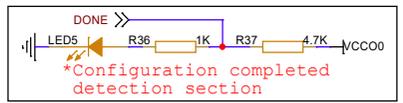
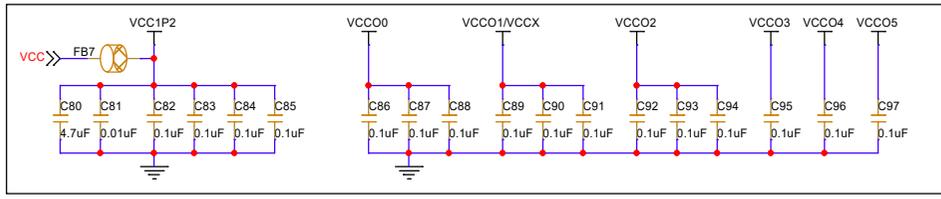
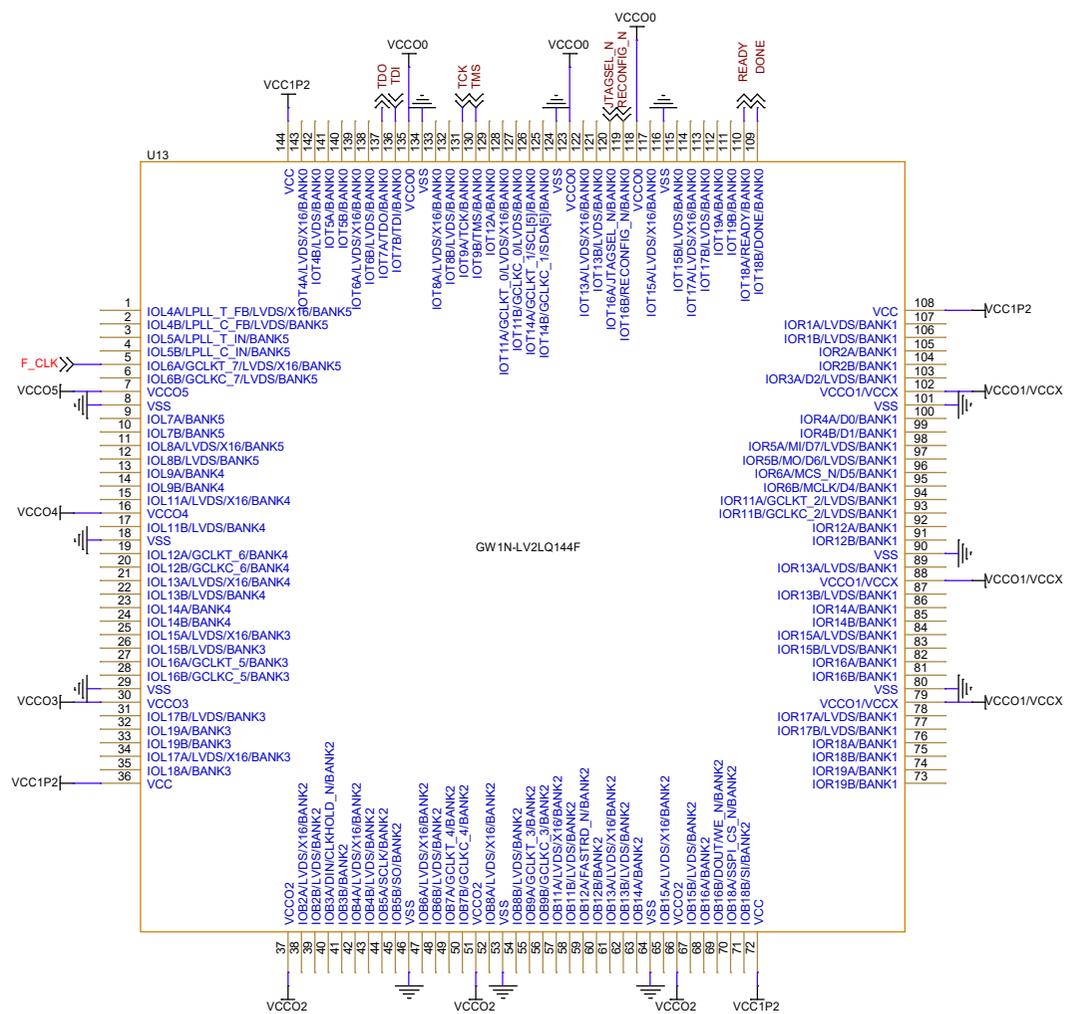


Notes:
 1.F CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

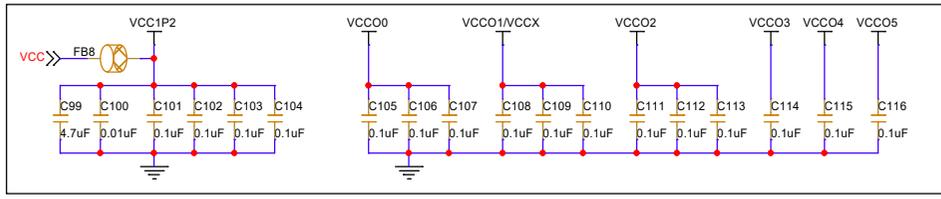
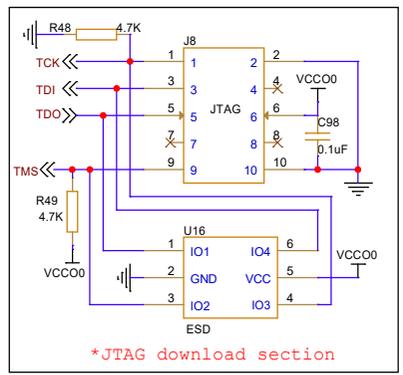
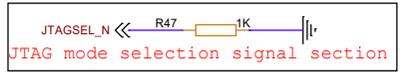
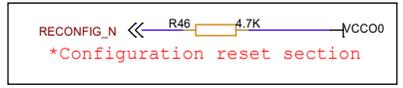
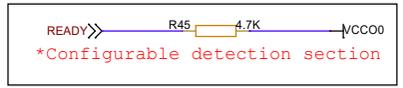
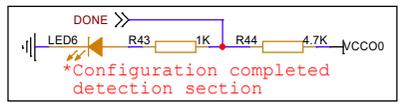
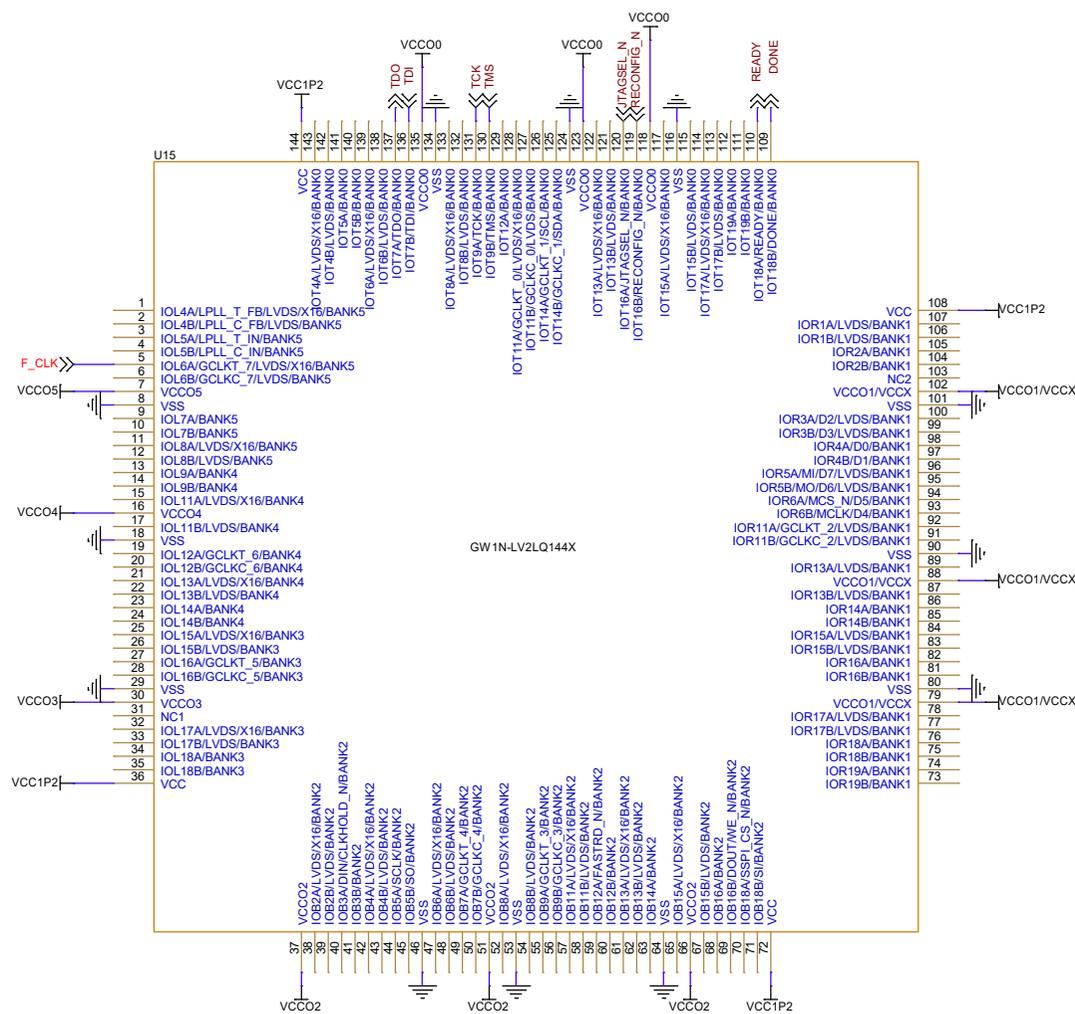
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Size	Document Number	Rev
B	GW1N-LV2LQ100X	2.1
Date:	Tuesday, April 09, 2024	Sheet 5 of 33



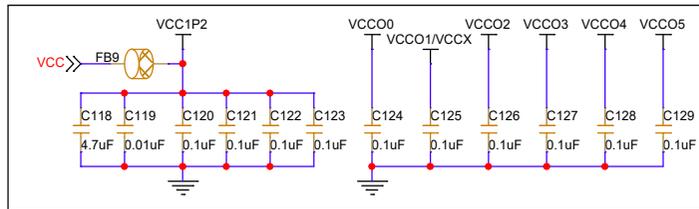
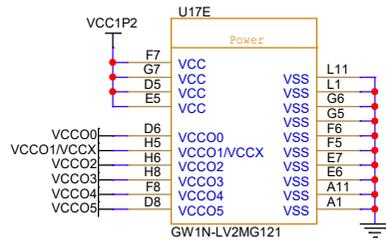
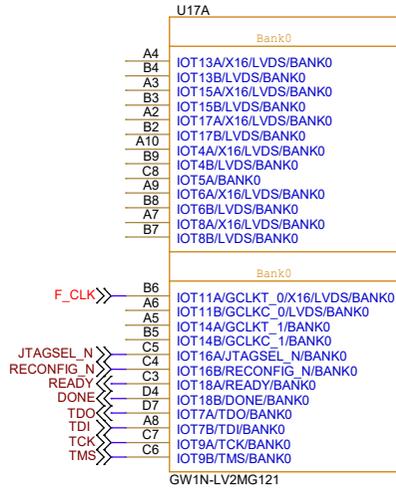
Notes:
 1.F_CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



Notes:
 1.F_CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

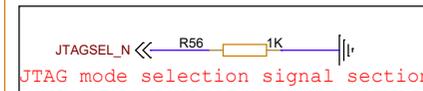
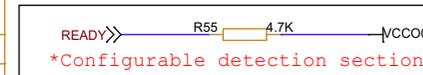
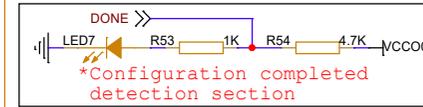
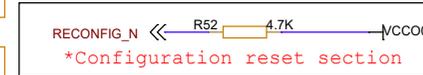
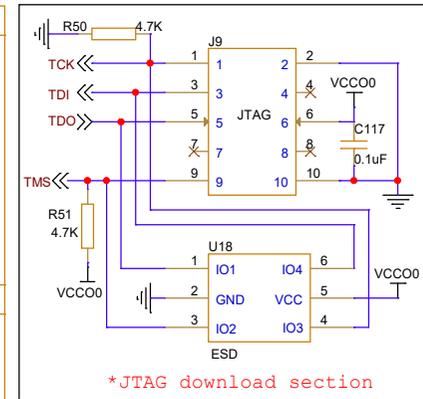
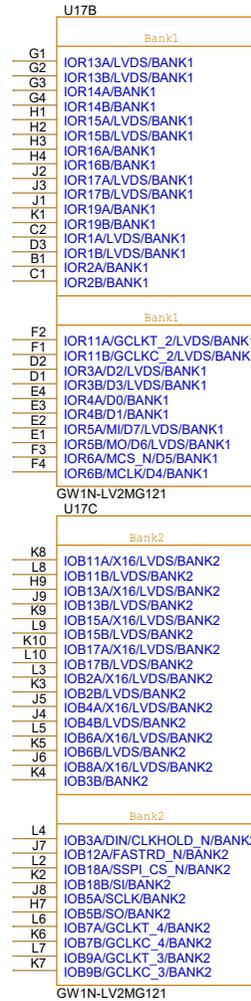
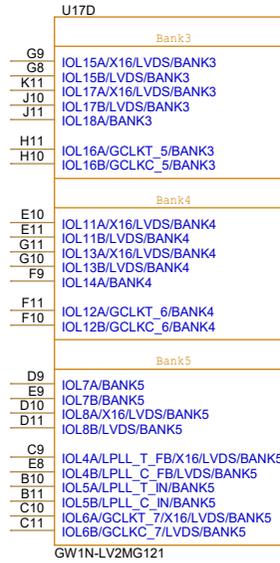


Notes:
 1.F_CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

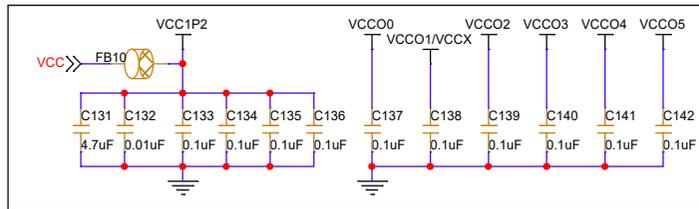
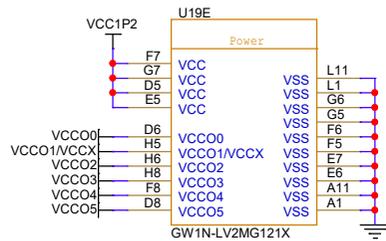
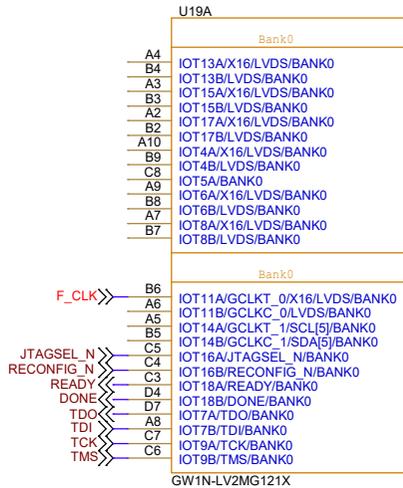


Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

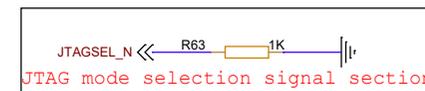
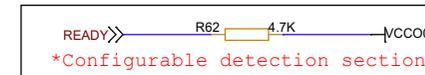
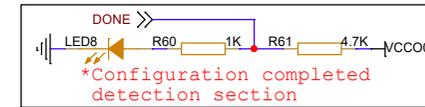
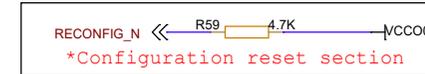
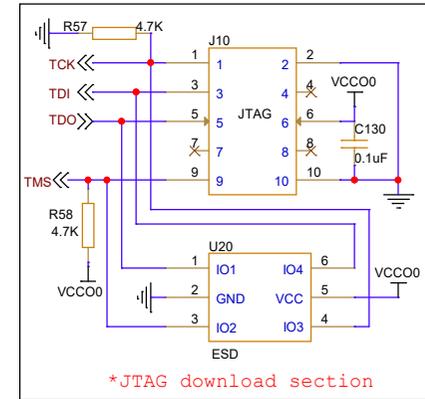
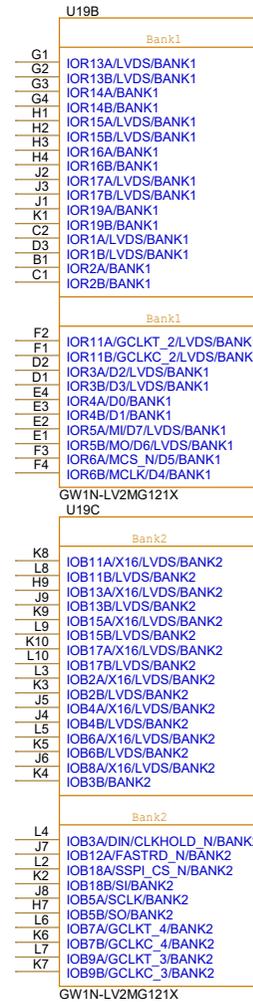
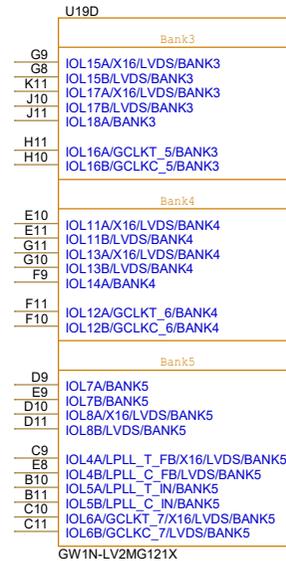


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GOWIN Minimum System Diagram		
Size	Document Number	Rev
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Date:	Tuesday, April 09, 2024	Sheet 9 of 33

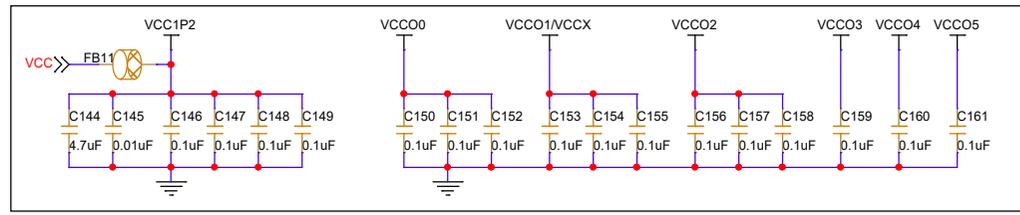
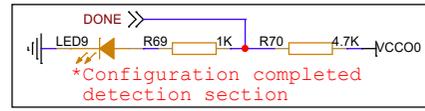
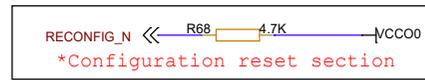
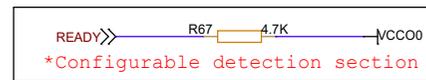
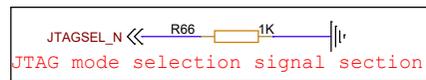
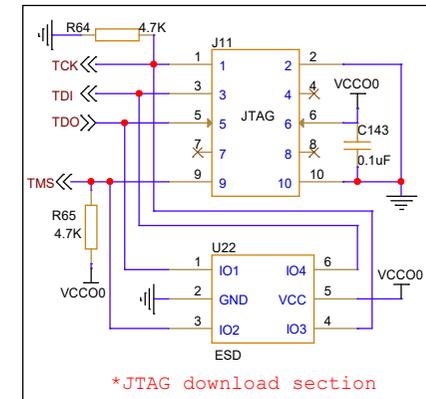
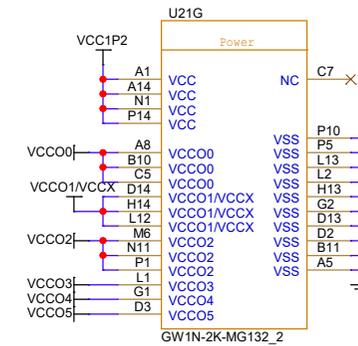
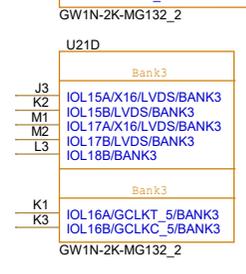
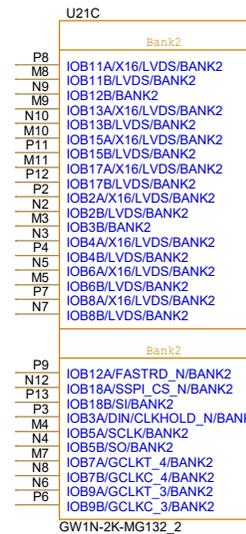
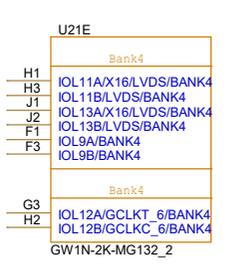
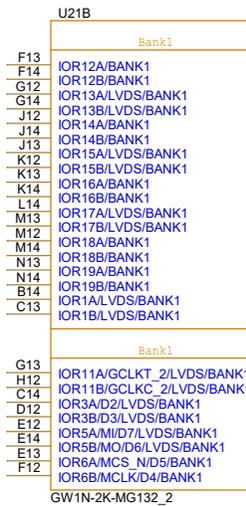
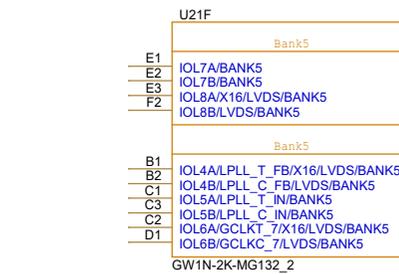
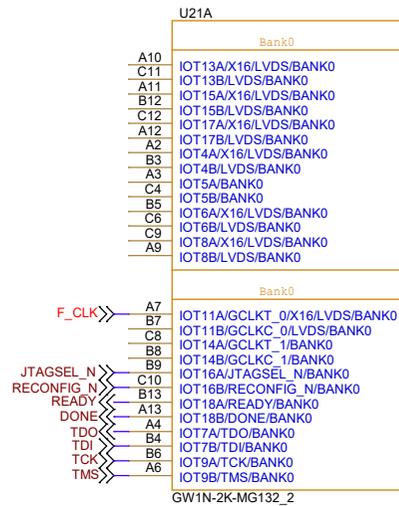


Notes:

- 1.F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection circuit to the JTAG download circuit.

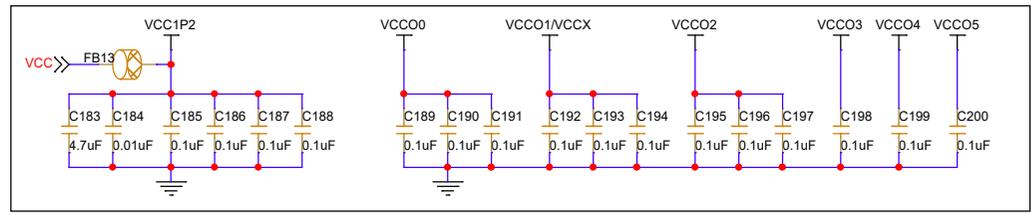
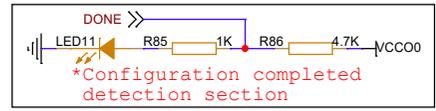
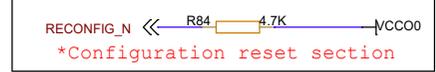
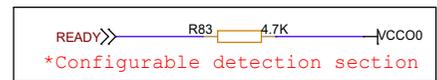
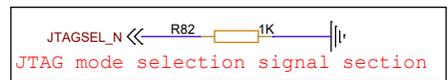
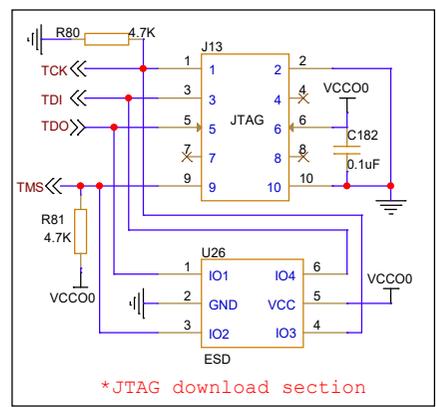
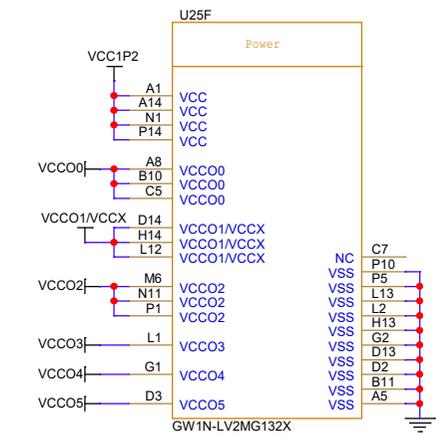
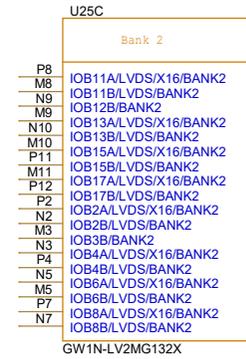
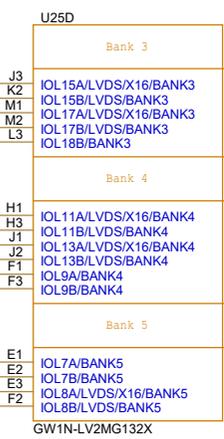
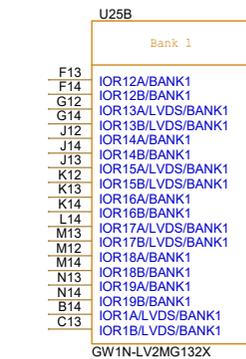
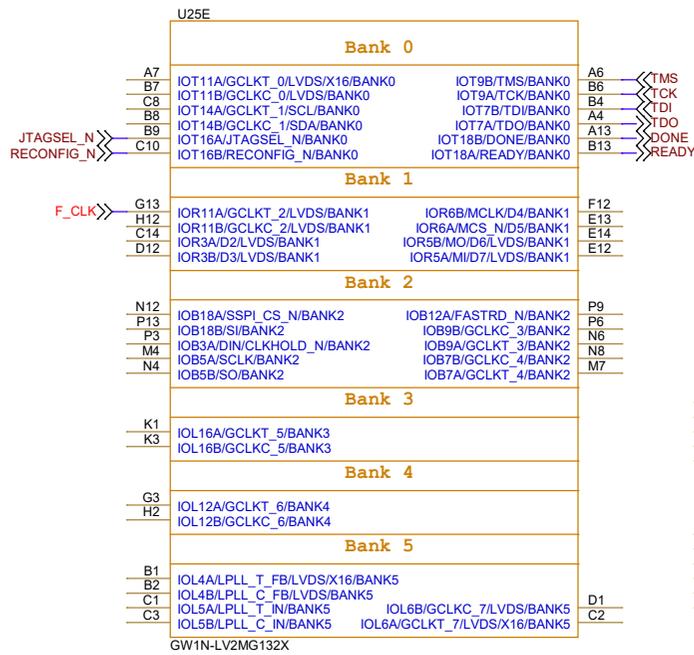


Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV2MG121X	2.1
Date:	Tuesday, April 09, 2024	Sheet 10 of 33



Notes:
 1.F CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

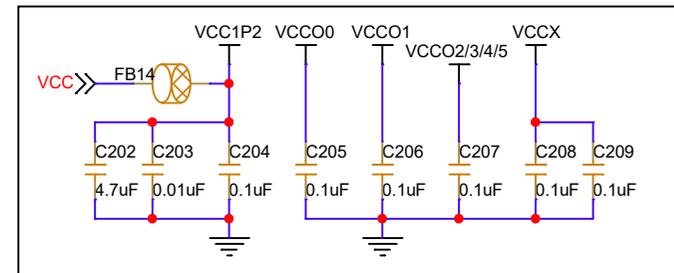
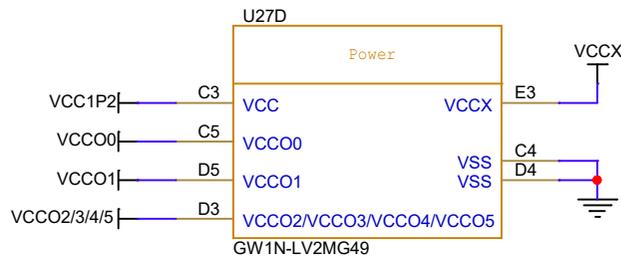
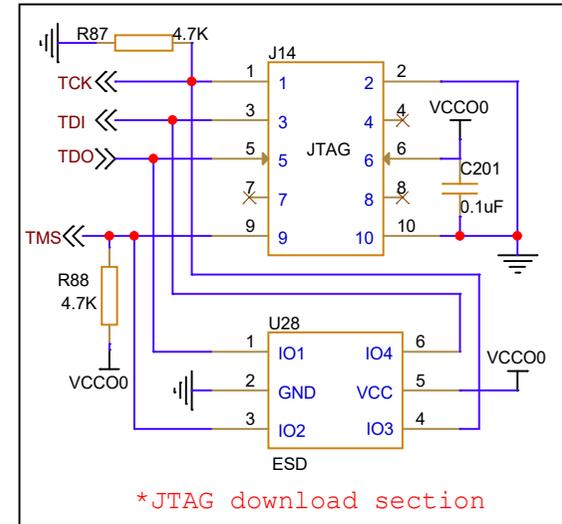
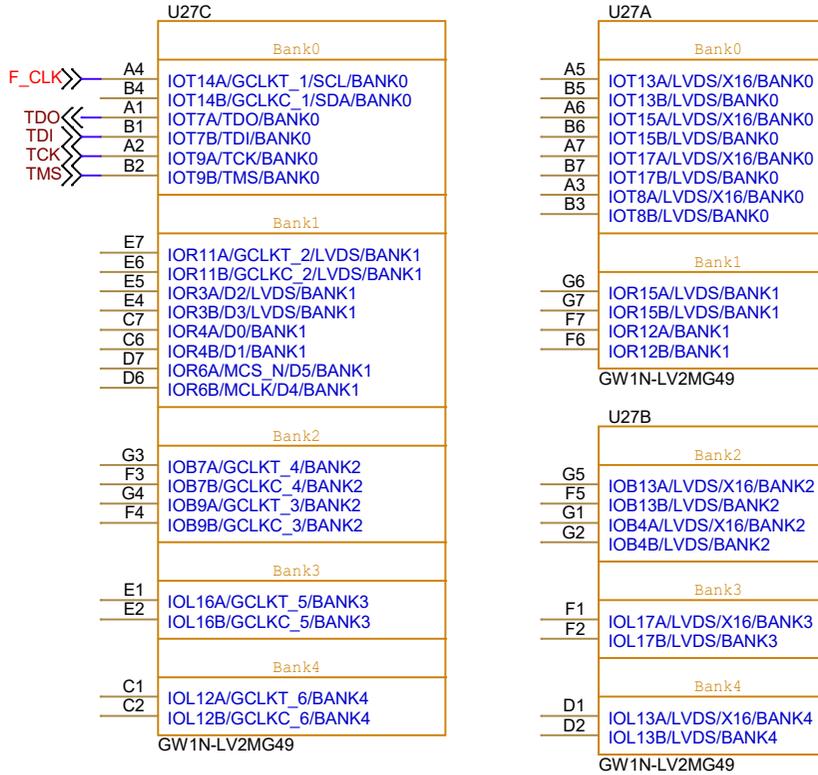
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV2MG132	2.1
Date:	Tuesday, April 09, 2024	Sheet 11 of 33



Notes:
 1. F CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV2MG132X	2.1
Date:	Tuesday, April 09, 2024	Sheet 13 of 33

GW1N-LV2MG49



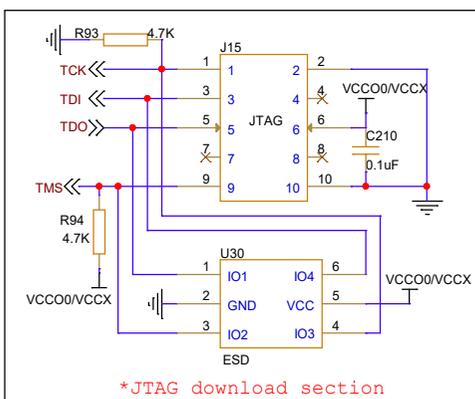
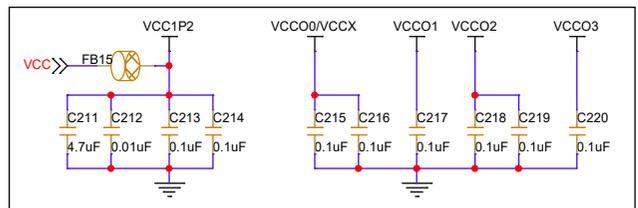
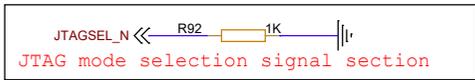
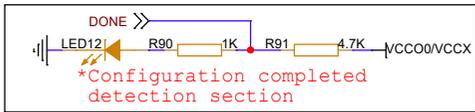
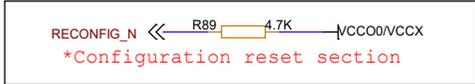
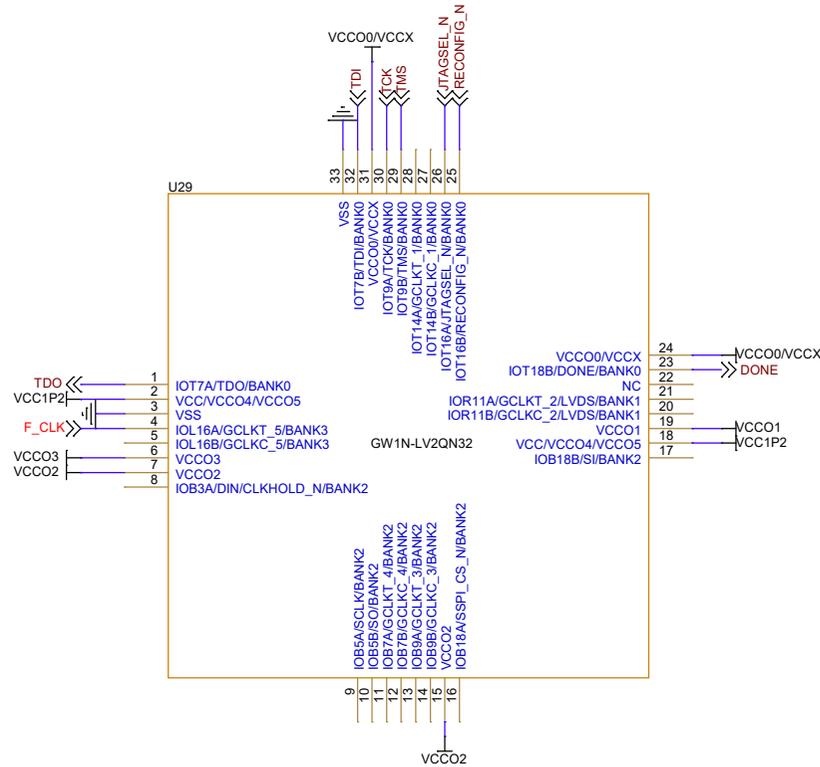
Notes:

1. F_CLK signal is an external input clock signal.

It is recommended that F_CLK signal be provided through an active oscillator crystal.

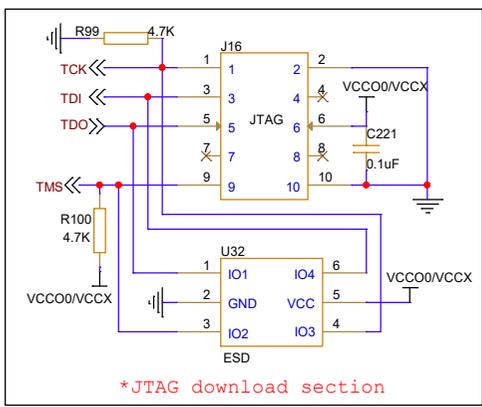
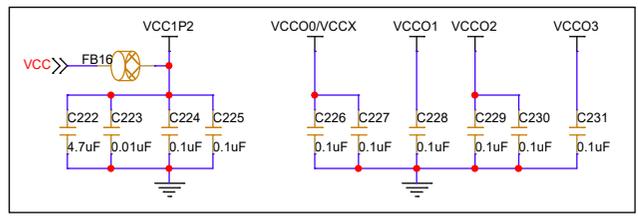
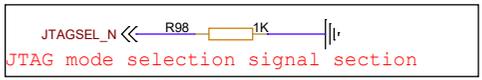
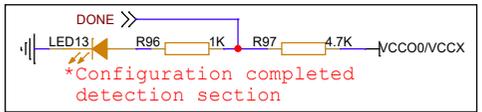
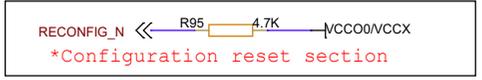
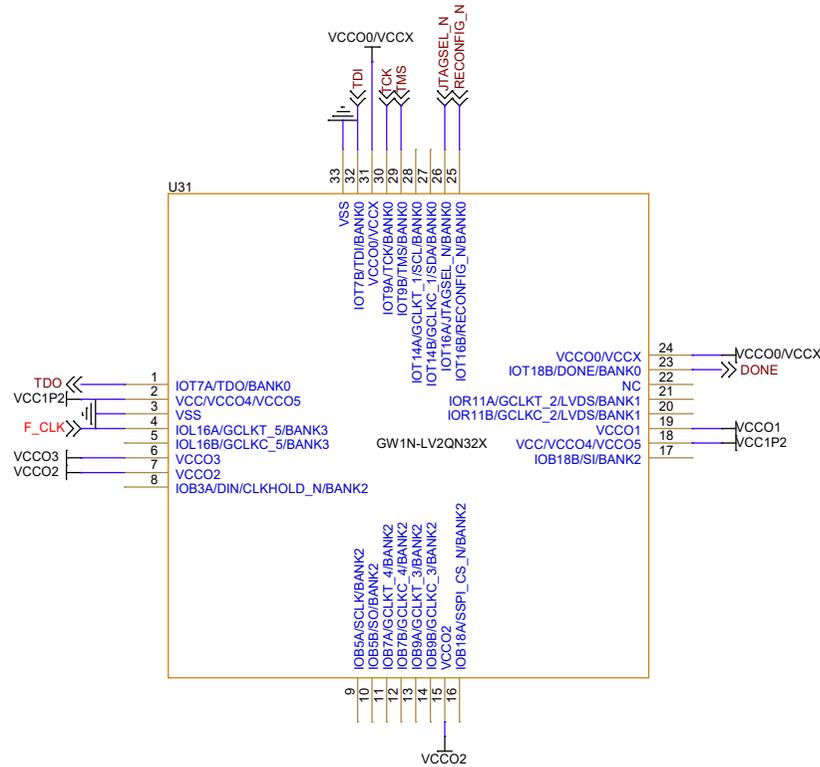
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
A4	GW1N-LV2MG49	2.1
Date:	Tuesday, April 09, 2024	Sheet 14 of 33



Notes:
 1. F_CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2. It is recommended that add an ESD protection chip to the JTAG download circuit.

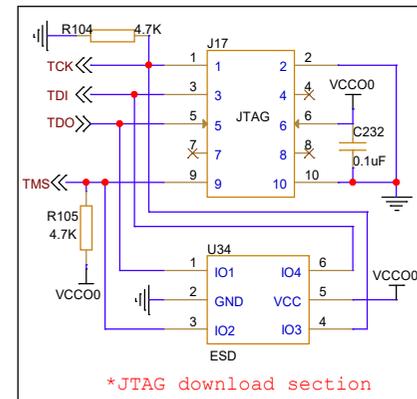
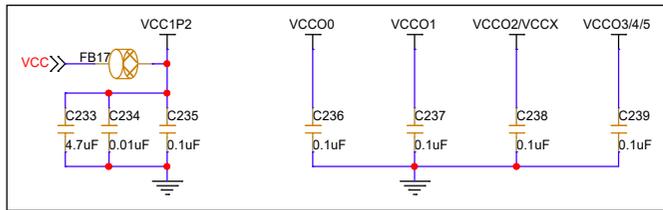
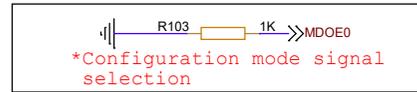
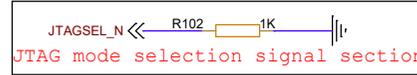
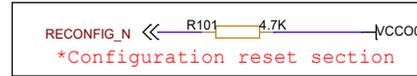
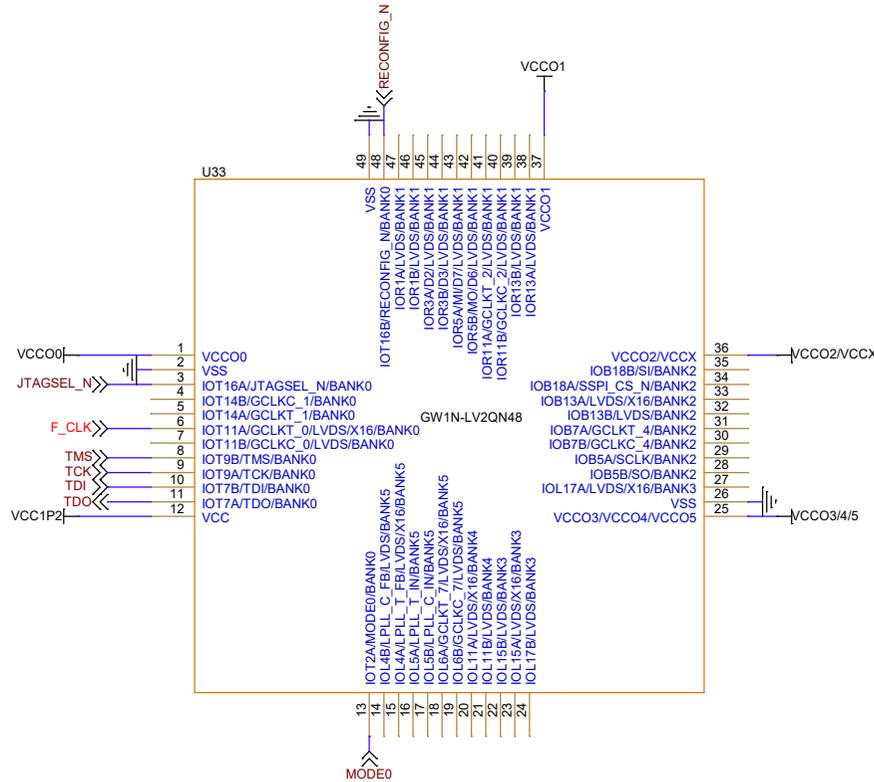
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV2QN32	2.1
Date:	Tuesday, April 09, 2024	Sheet 15 of 33



Notes:
 1. F CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV2QN32X	2.1
Date:	Tuesday, April 09, 2024	Sheet 16 of 33

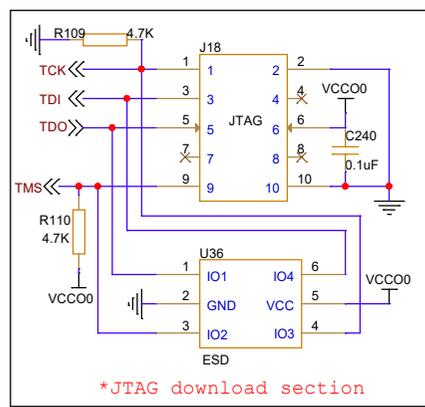
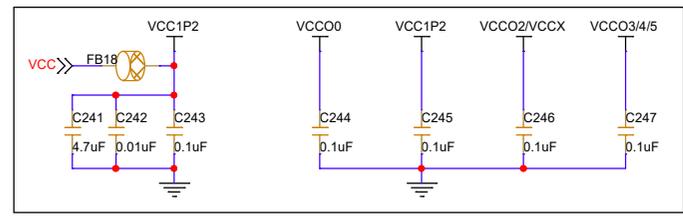
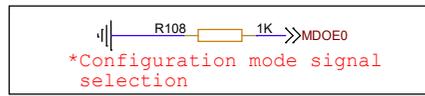
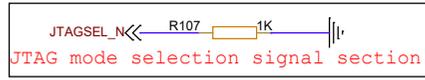
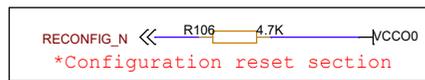
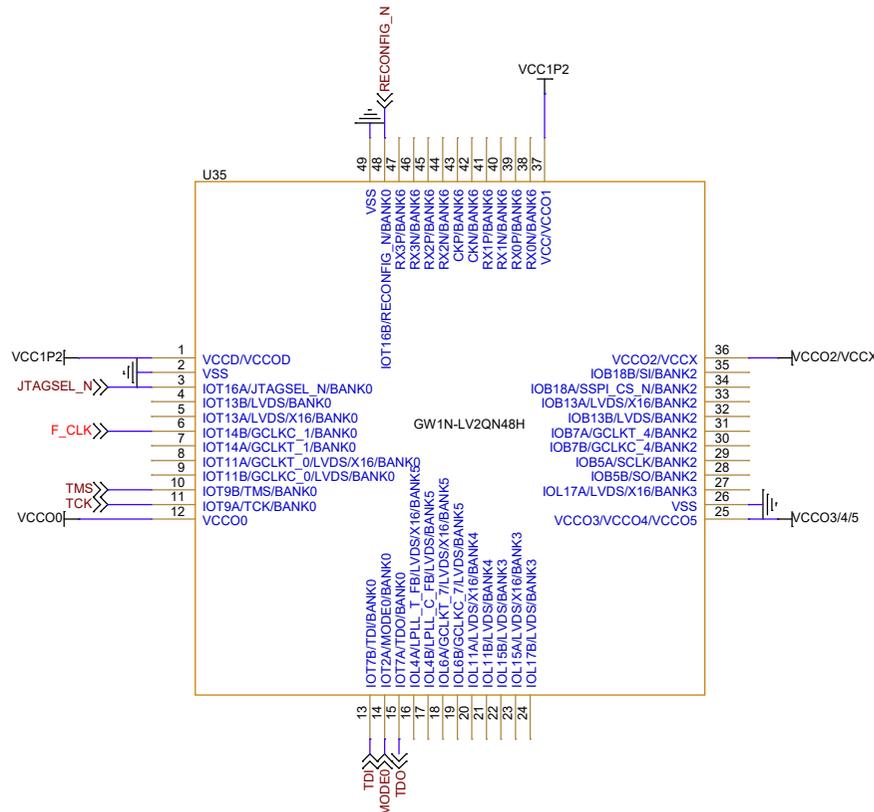
GW1N-LV2QN48



Notes:

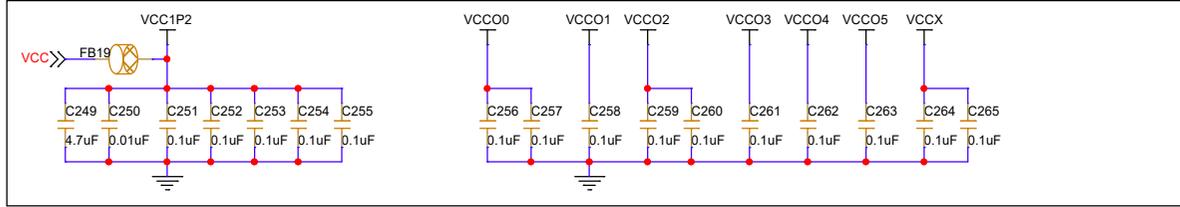
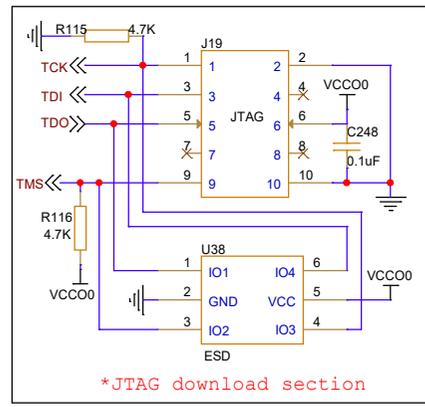
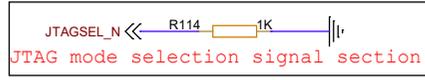
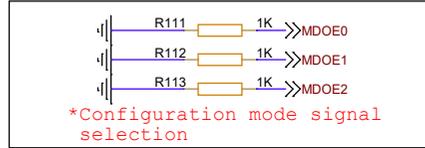
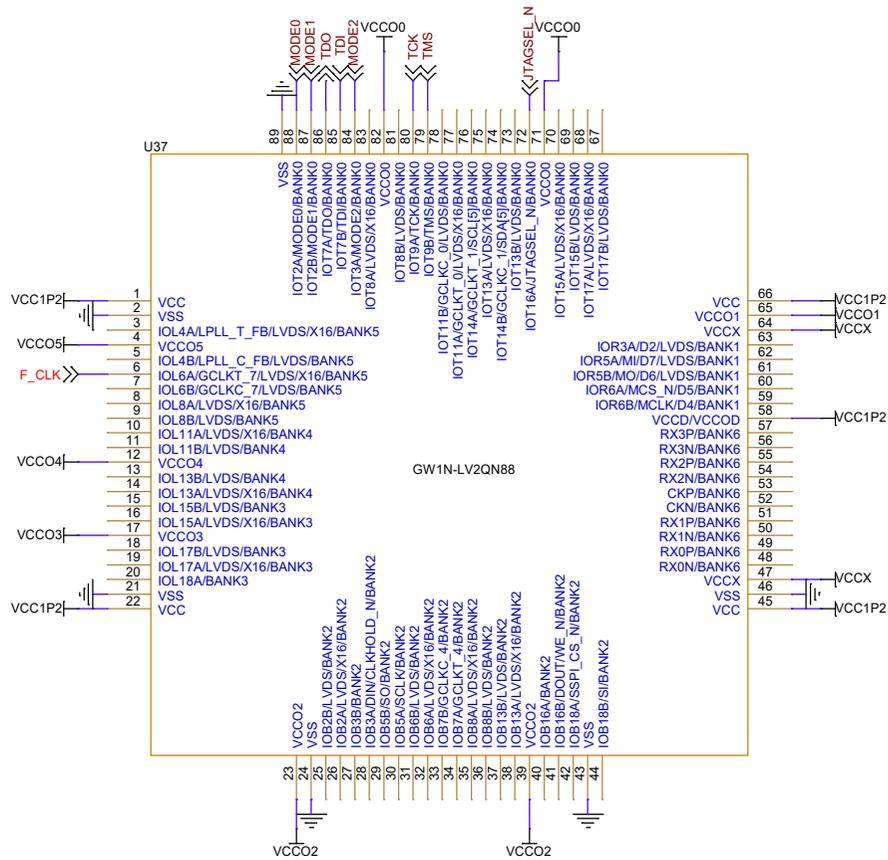
- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-LV2QN48	2.1
Date:	Tuesday, April 09, 2024	Sheet 17 of 33



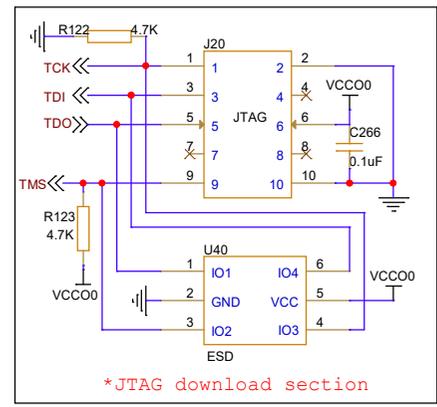
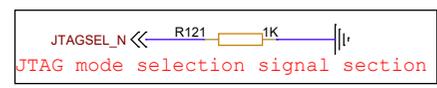
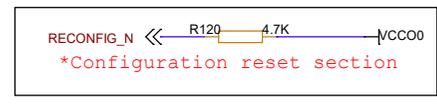
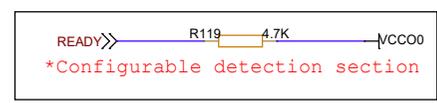
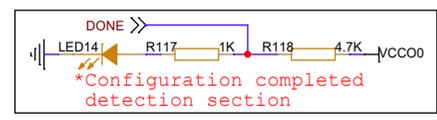
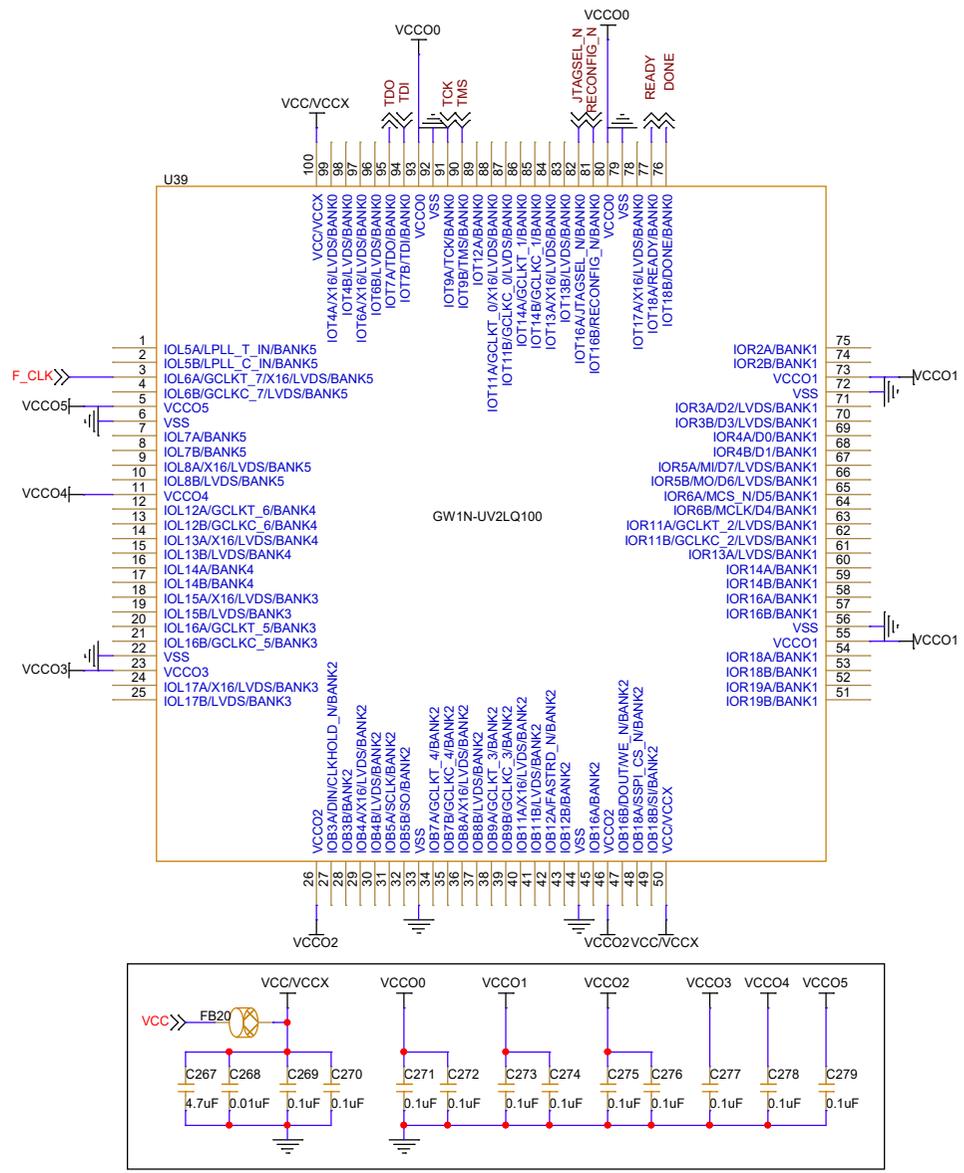
Notes:
 1. F_CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number	Rev
	GW1N-LV2QN48H	2.1
Date:	Wednesday, April 10, 2024	Sheet 18 of 33



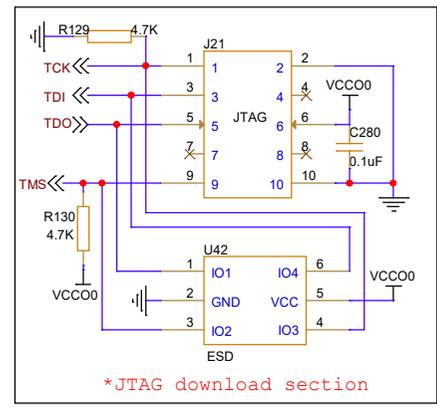
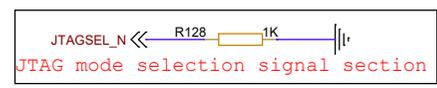
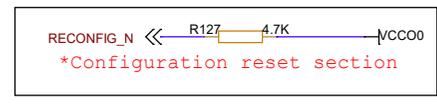
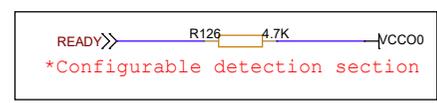
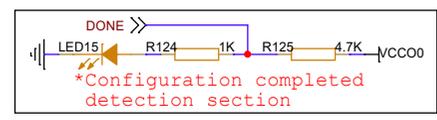
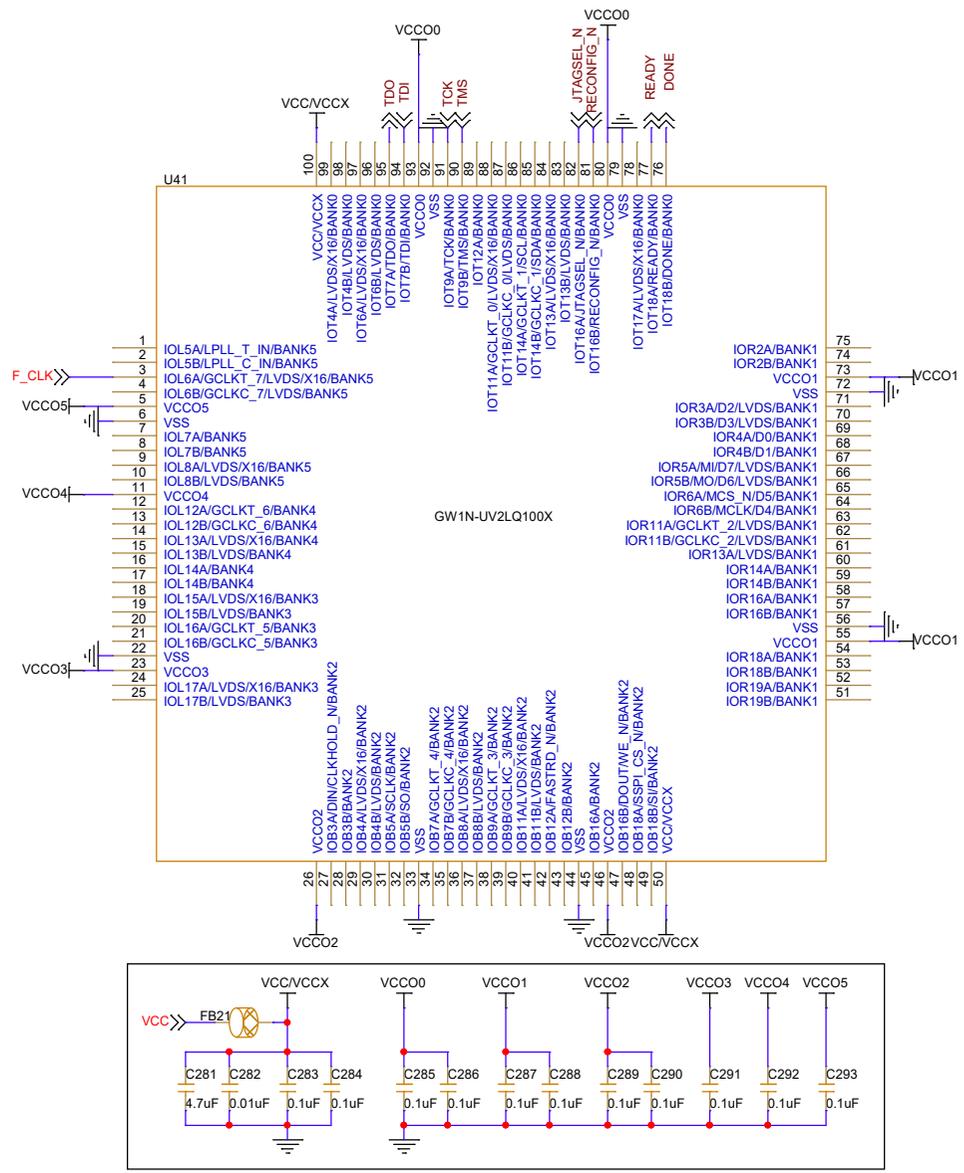
Notes:
 1.F CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number	Rev
	GW1N-LV2QN88	2.1
Date:	Tuesday, April 09, 2024	Sheet 19 of 33



Notes:
 1. F_CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2. It is recommended that add an ESD protection chip to the JTAG download circuit.

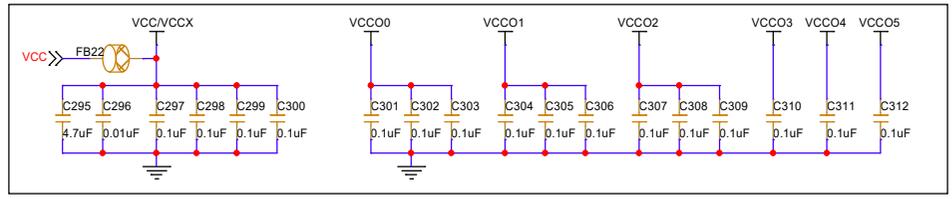
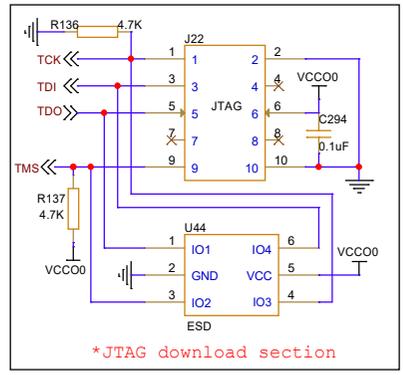
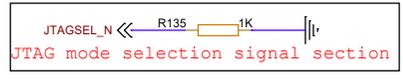
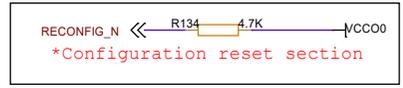
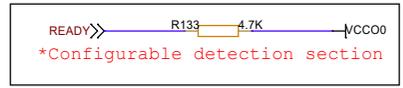
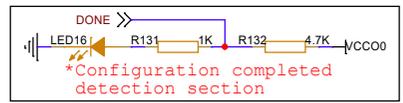
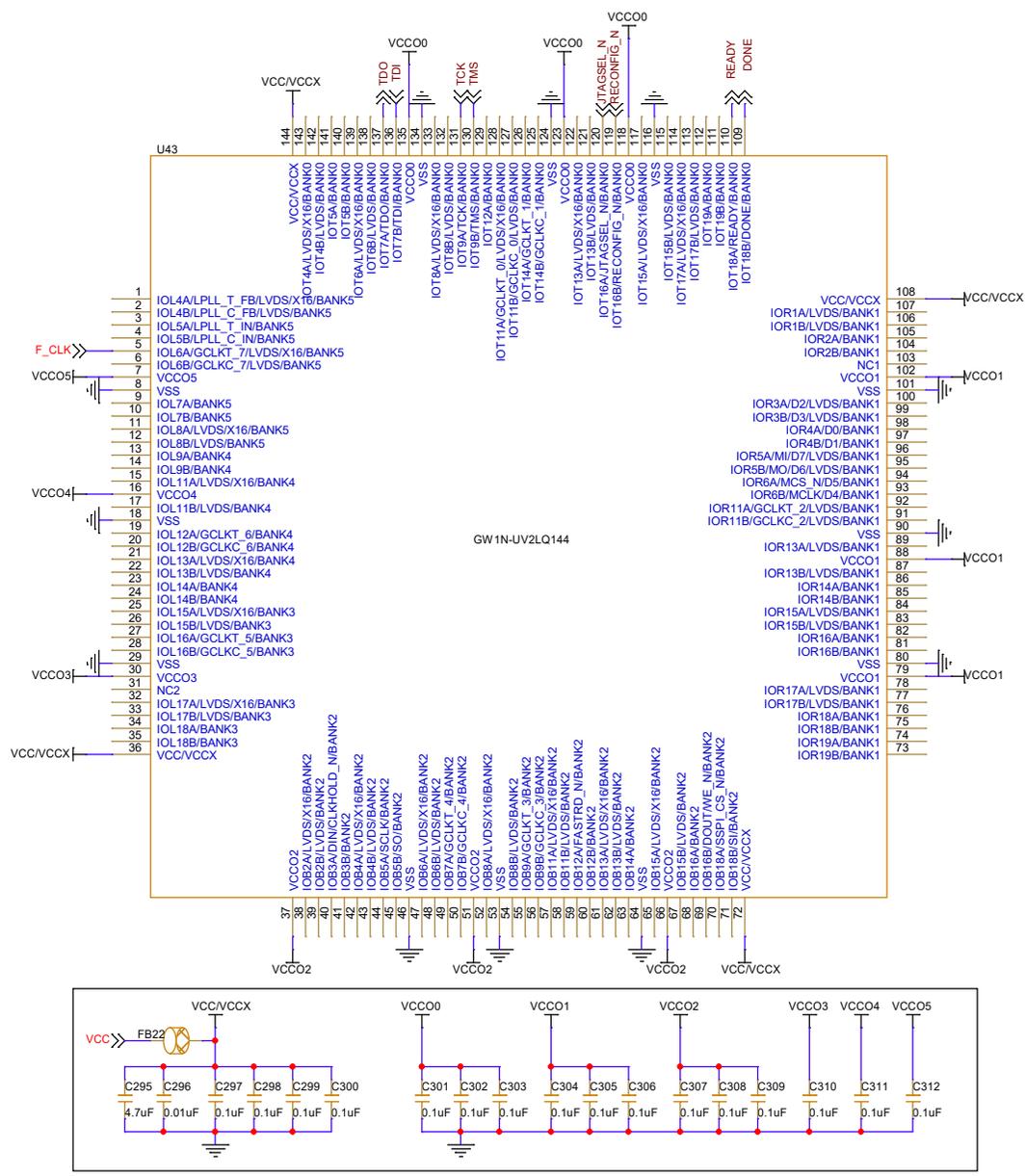
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GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV2LQ100	2.1
Date:	Tuesday, April 09, 2024	Sheet 20 of 33



Notes:

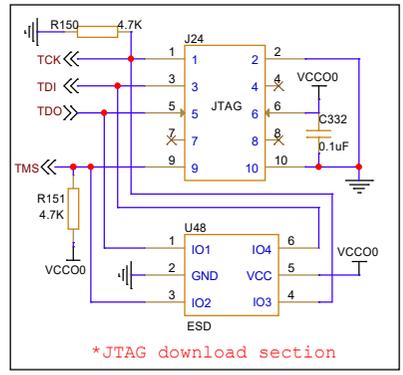
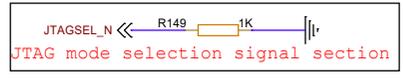
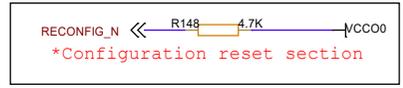
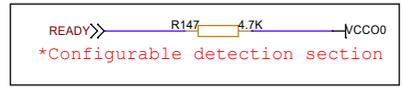
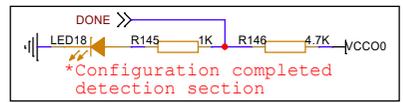
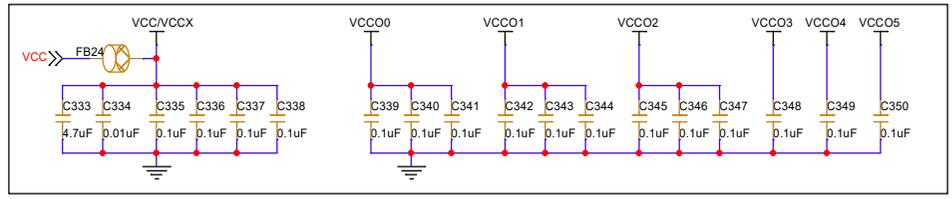
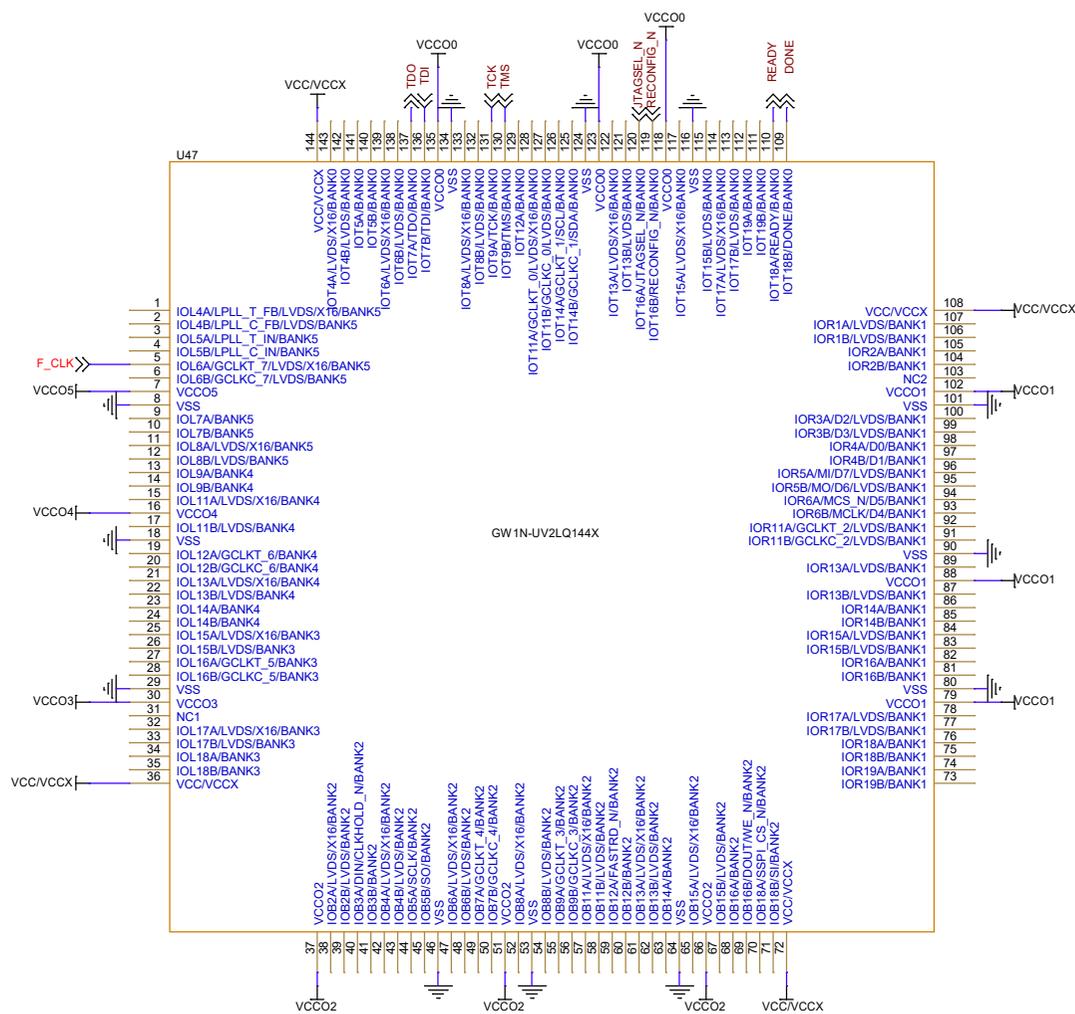
- 1.F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV2LQ100X	2.1
Date:	Tuesday, April 09, 2024	Sheet 21 of 33

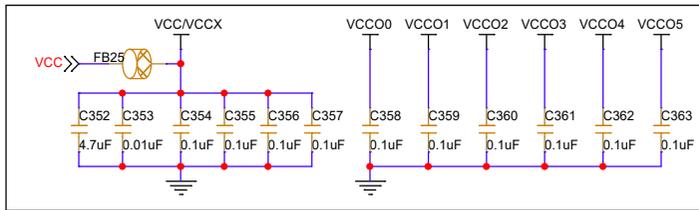
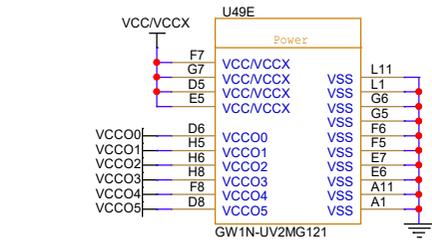
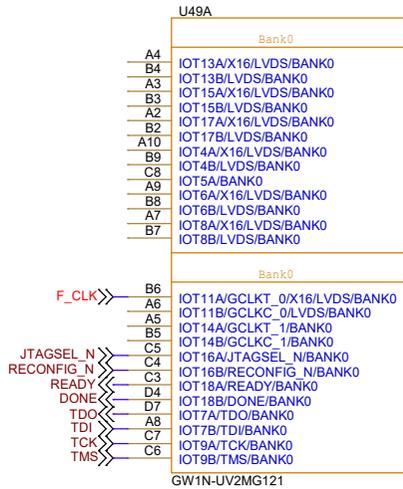


Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

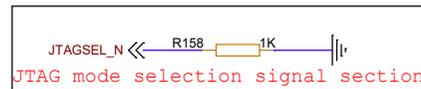
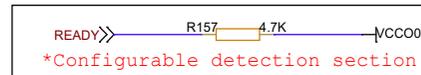
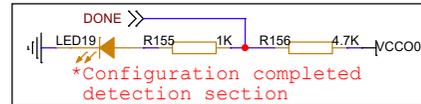
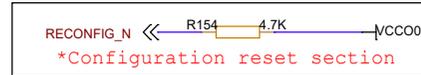
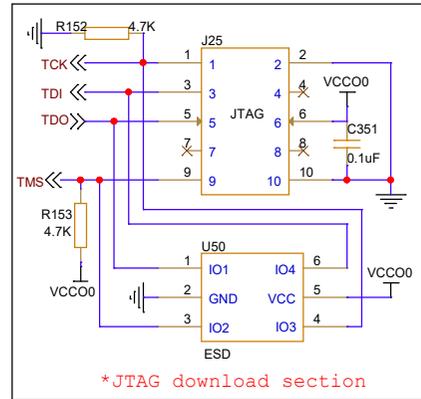
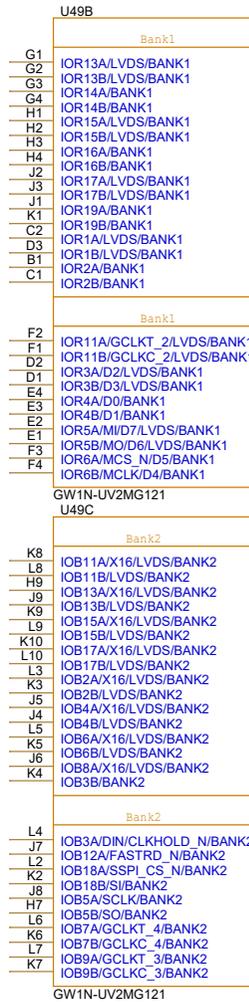
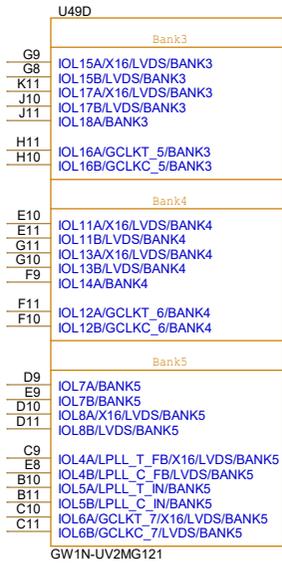


Notes:
 1.F CLK signal is an external input clock signal.
 It is recommended that F CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

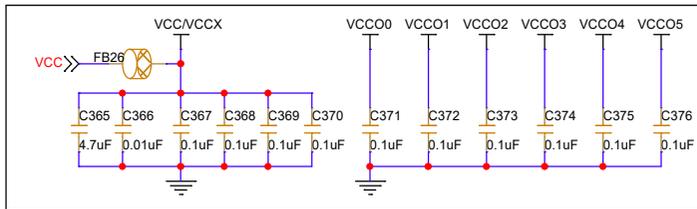
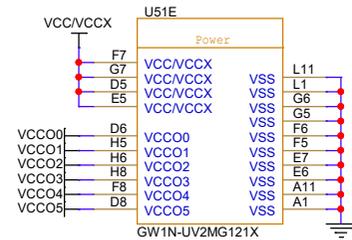
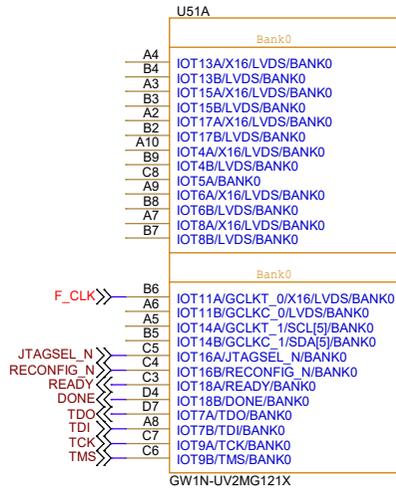


Notes:

- 1.F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

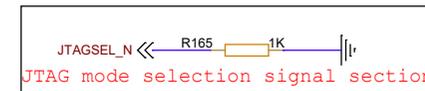
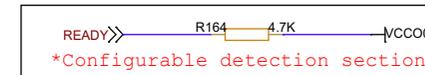
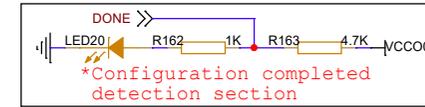
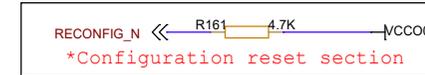
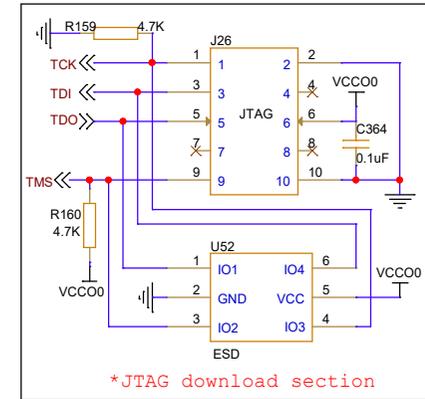
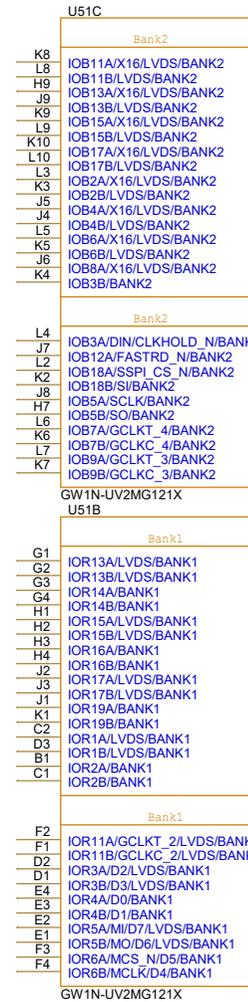
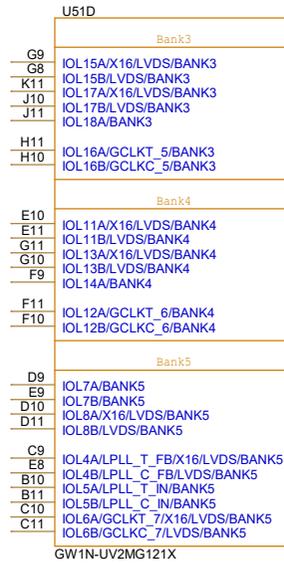


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GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV2MG121	2.1
Date:	Tuesday, April 09, 2024	Sheet 25 of 33

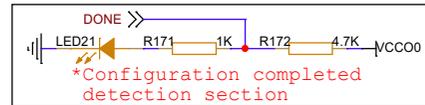
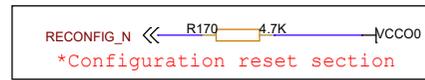
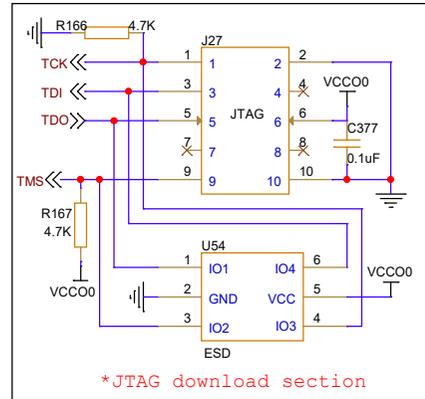
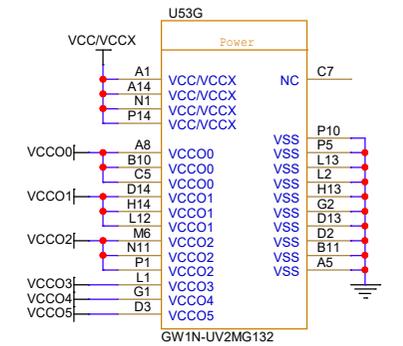
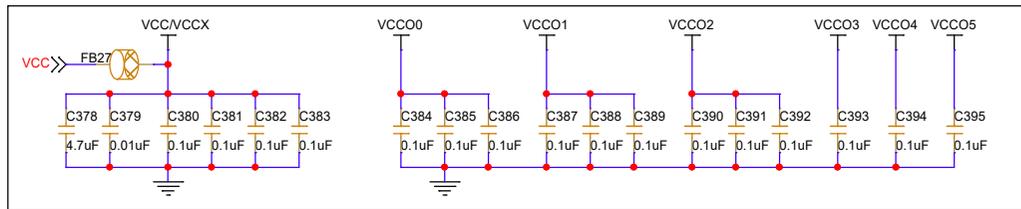
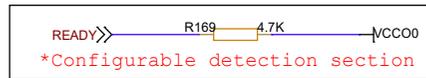
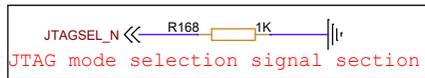
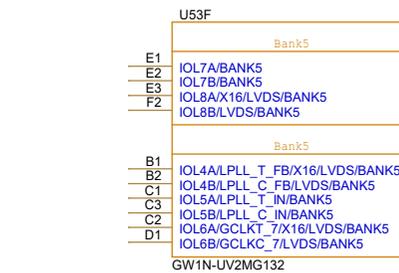
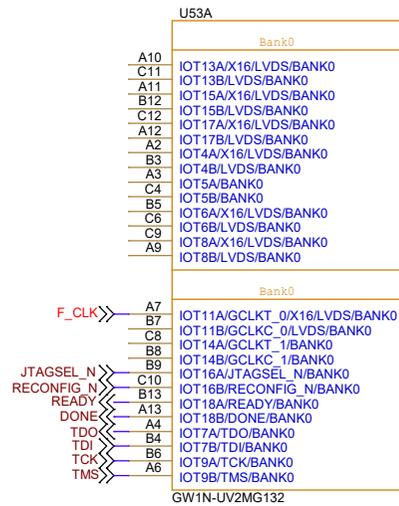


Notes:

- 1.F_CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.



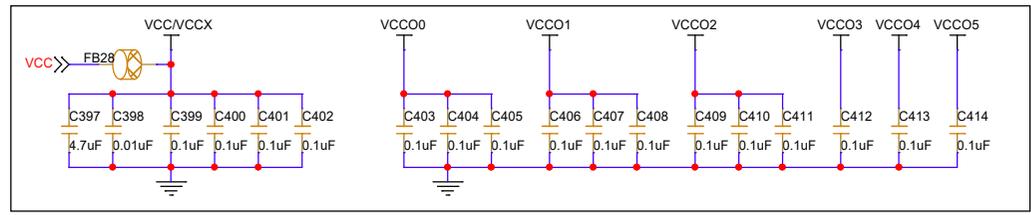
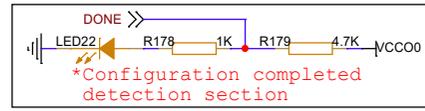
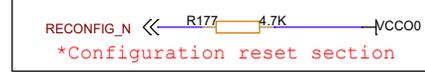
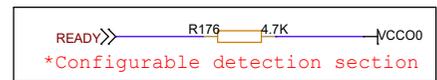
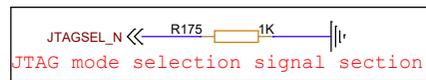
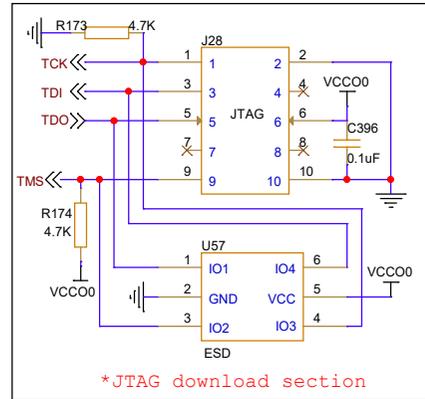
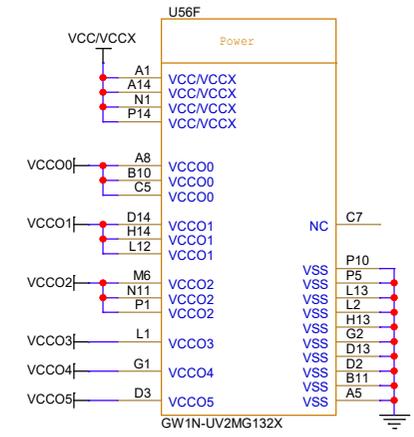
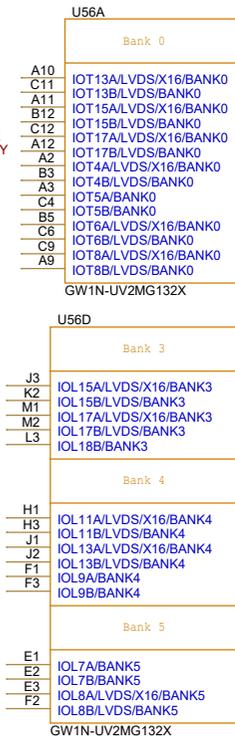
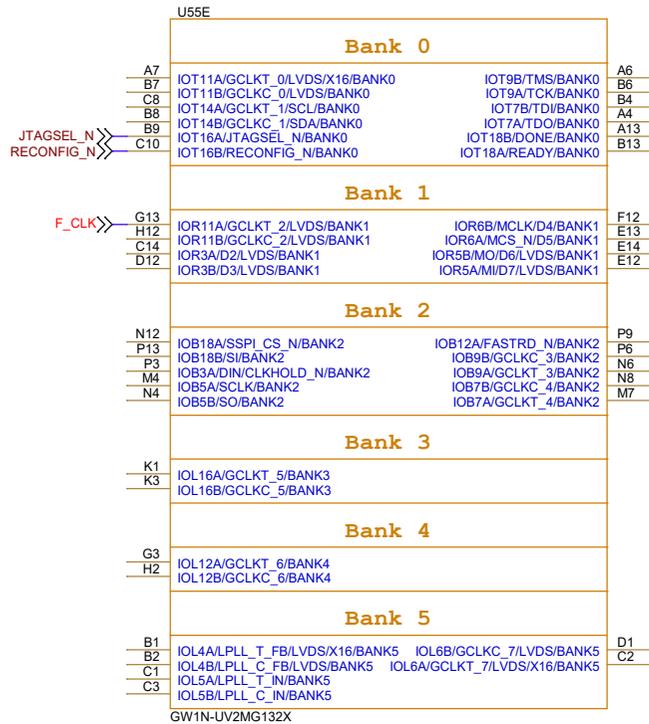
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV2MG121X	2.1
Date:	Tuesday, April 09, 2024	Sheet 26 of 33



Notes:

- 1.F CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

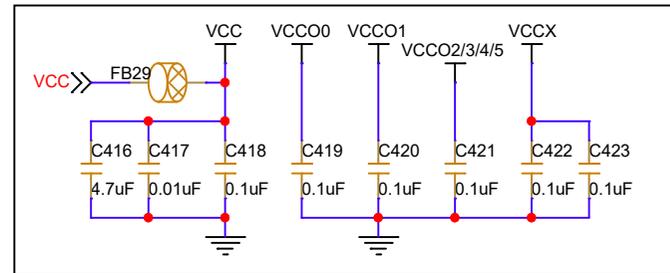
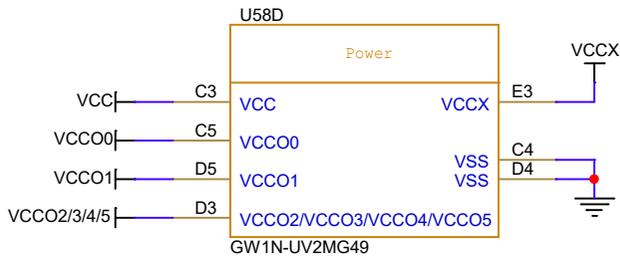
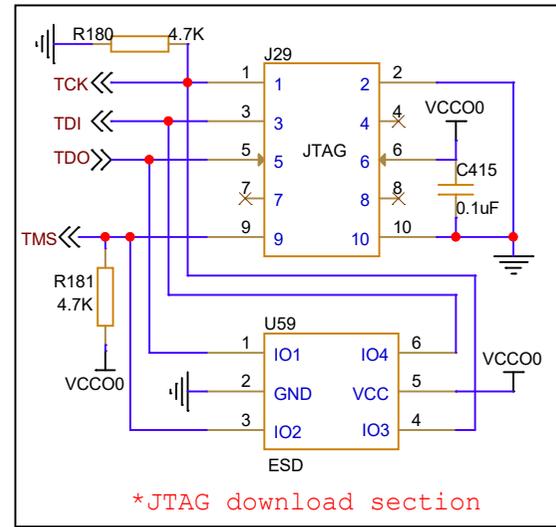
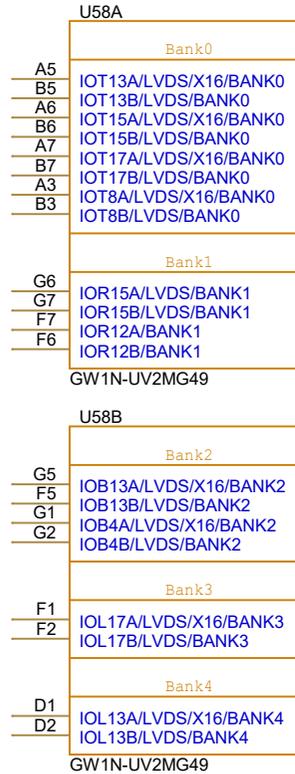
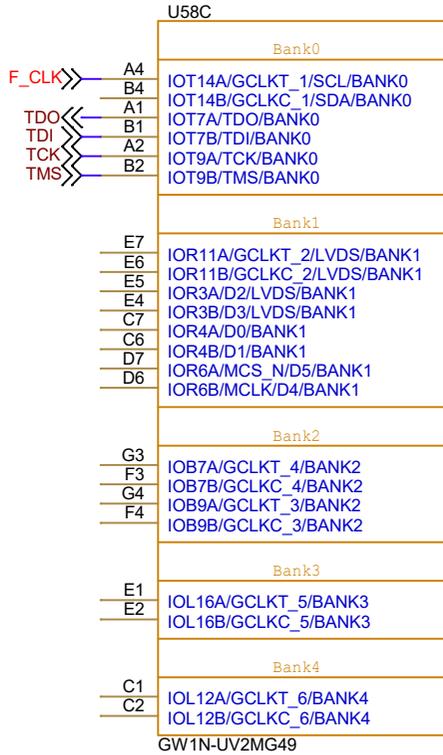
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GOWIN Minimum System Diagram		
Size B	Document Number GW1N-UV2MG132	Rev 2.1
Date: Tuesday, April 09, 2024	Sheet 27 of 33	



Notes:
 1.F CLK signal is an external input clock signal.
 It is recommended that F_CLK signal be provided through an active oscillator crystal.
 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV2MG132X	2.1
Date:	Tuesday, April 09, 2024	Sheet 28 of 33

GW1N-UV2MG49

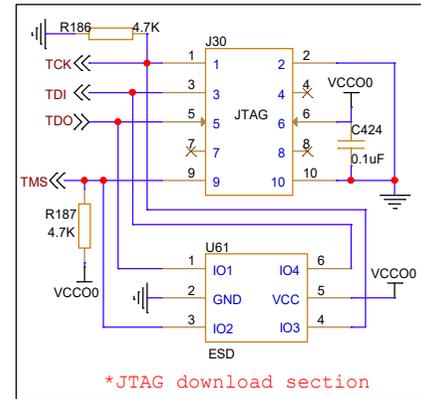
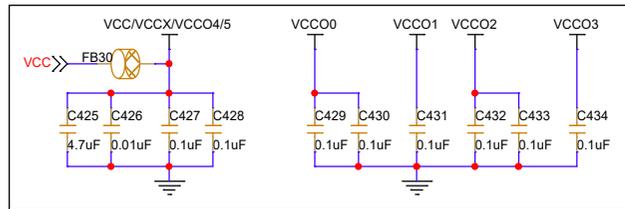
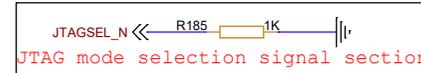
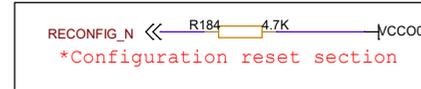
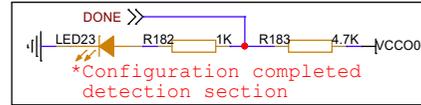
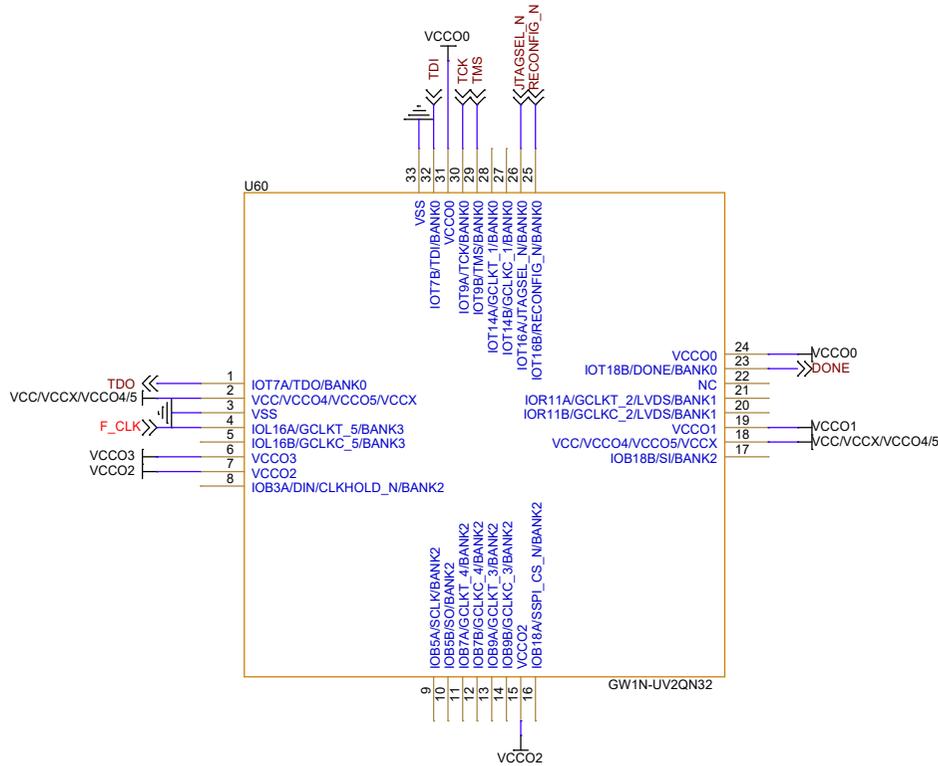


Notes:

1. F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

Title GOWIN Minimum System Diagram		
Size A4	Document Number GW1N-UV2MG49	Rev 2.1
Date: Tuesday, April 09, 2024	Sheet 29	of 33

GW1N-UV2QN32

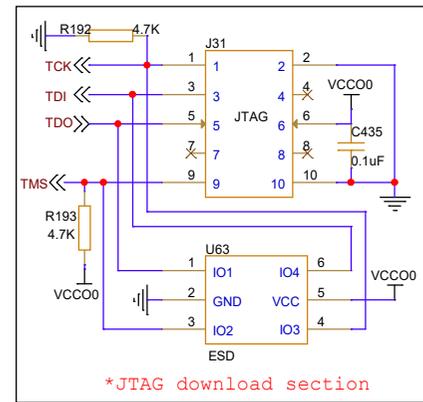
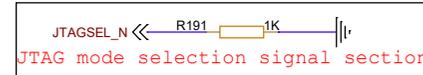
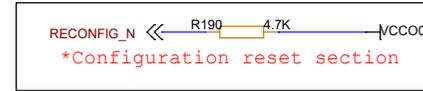
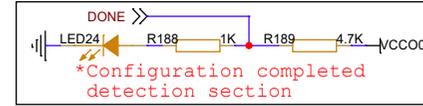
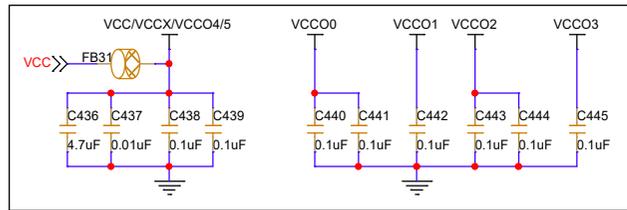
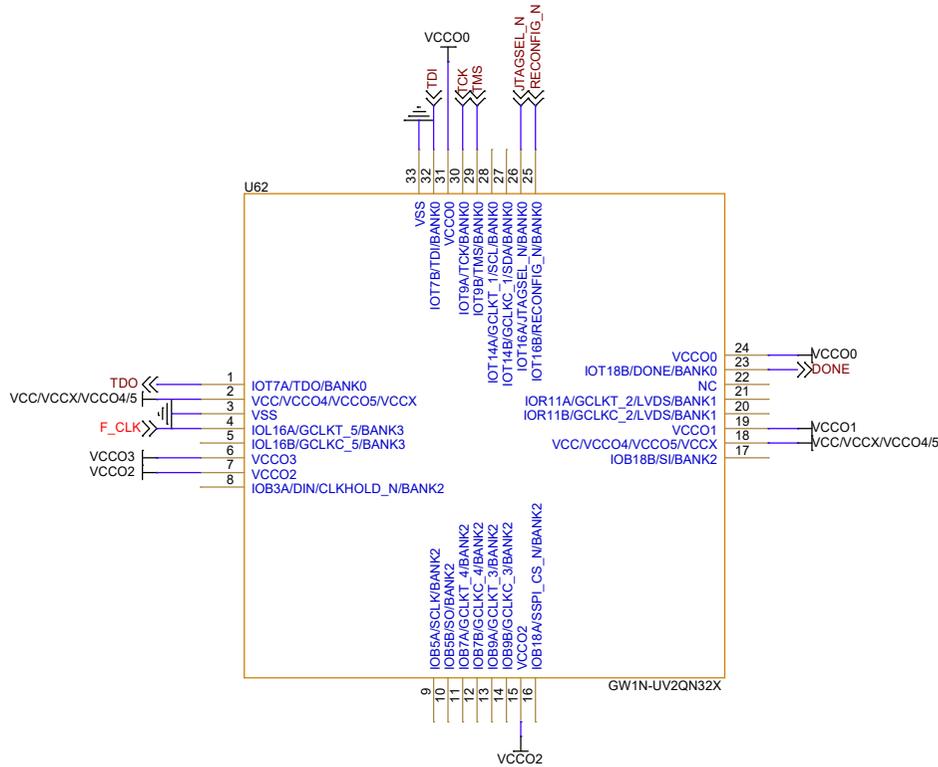


Notes:

- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
- 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV2QN32	2.1
Date:	Tuesday, April 09, 2024	Sheet 30 of 33

GW1N-UV2QN32X

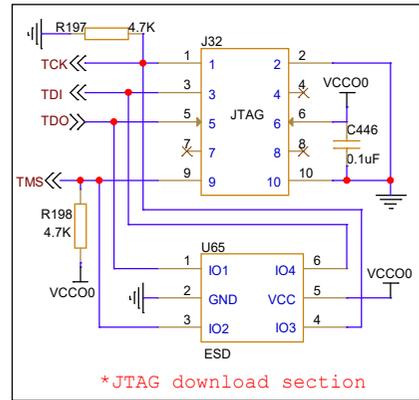
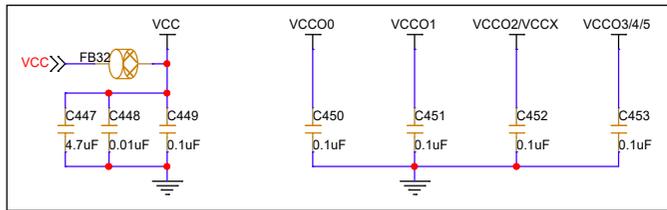
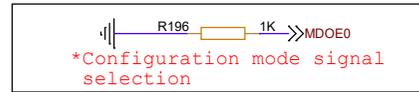
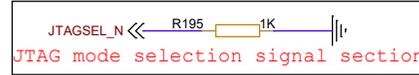
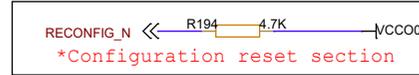
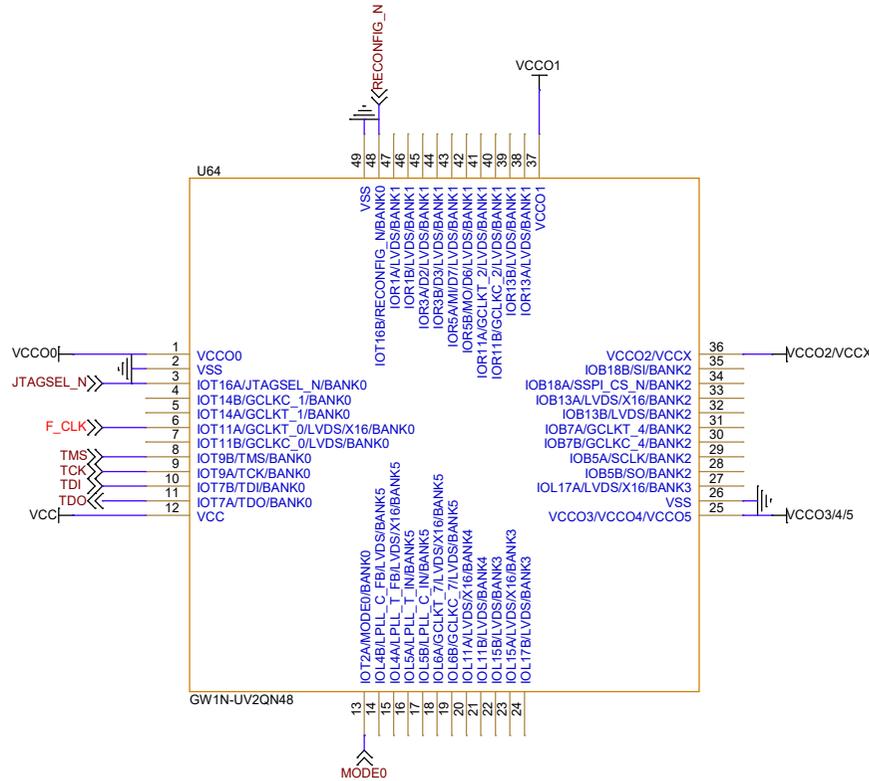


Notes:

1. F_CLK signal is an external input clock signal. It is recommended that F_CLK signal be provided through an active oscillator crystal.
2. It is recommended that add an ESD protection chip to the JTAG download circuit.

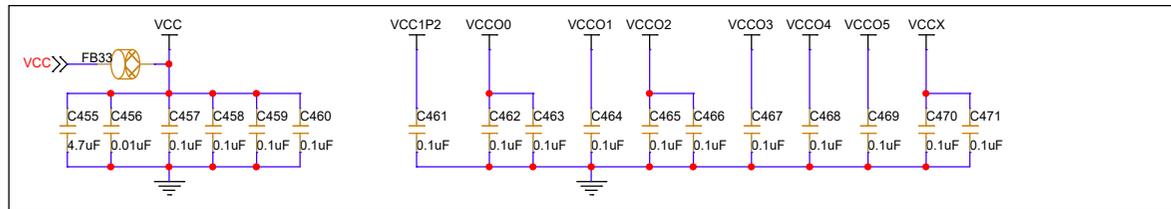
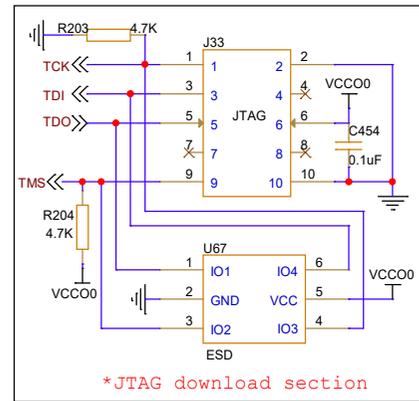
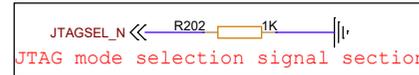
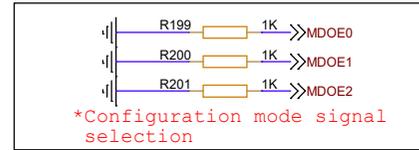
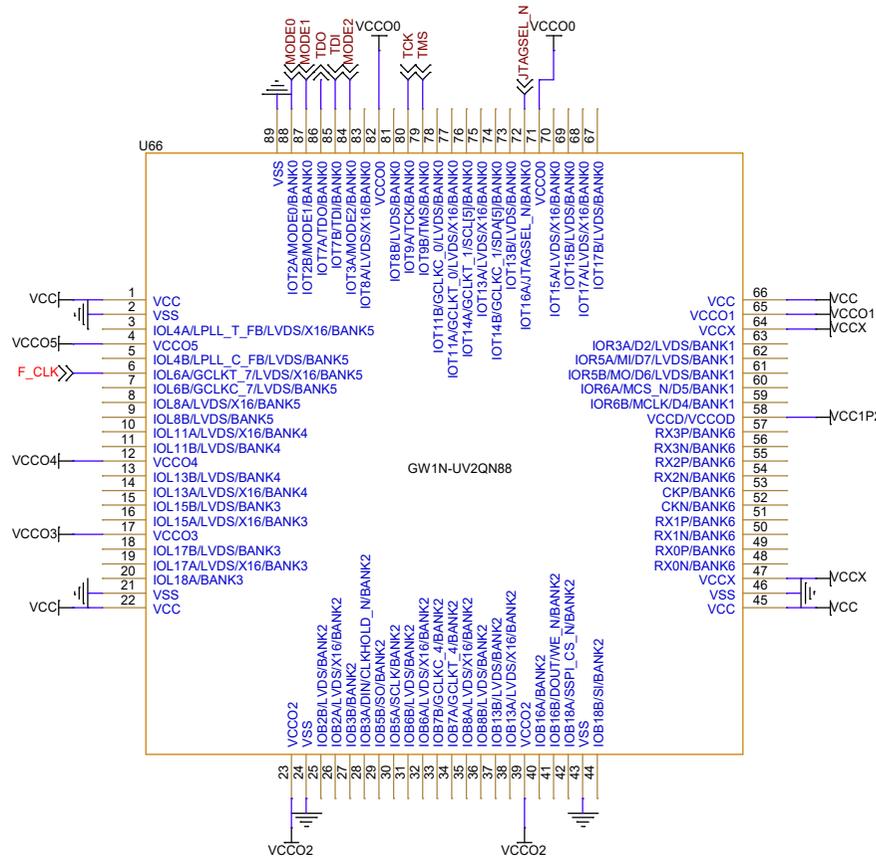
Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV2QN32X	2.1
Date:	Tuesday, April 09, 2024	Sheet 31 of 33

GW1N-UV2QN48



- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size	Document Number	Rev
B	GW1N-UV2QN48	2.1
Date:	Tuesday, April 09, 2024	Sheet 32 of 33



- Notes:
- 1.F CLK signal is an external input clock signal.
It is recommended that F_CLK signal be provided through an active oscillator crystal.
 - 2.It is recommended that add an ESD protection chip to the JTAG download circuit.

Title		
GOWIN Minimum System Diagram		
Size B	Document Number	Rev
	GW1N-UV2QN88	2.1
Date:	Tuesday, April 09, 2024	Sheet 33 of 33