DK_VIDEO_GW2A-LV18PG484C8I7_V1.2

User Guide

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1 About This Guide

1.1 Purpose

The DK_VIDEO_GW2A-LV18PG484C8I7_V1.2 development board (hereinafter referred to development board) user guide consists of following three parts:

- A brief introduction to the function features of the development board;
- An introduction to the system architecture and hardware resources of the development board;
- An introduction to the functions, circuits, and pinouts of each module.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS102, GW2A series of FPGA Products Data Sheet
2. UG110, GW2A-18 Pinout
3. UG111, GW2A series of FPGA Products Package and Pinout Manual

1.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Abbreviations and Terminology

Terminology and Abbreviations	Meaning
BSRAM	Block Static Random Access Memory
DDR	Double-Data-Rate Synchronous Dynamic Random Access Memory
DSP	Digital Signal Processing
FLASH	Flash Memory

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPIO	Gowin Programmable Input/Output
LDO	Low Dropout Regulator
LUT4	4-input Look-up Tables
LVDS	Low-Voltage Differential Signaling
SSRAM	Shadow Static Random Access Memory

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

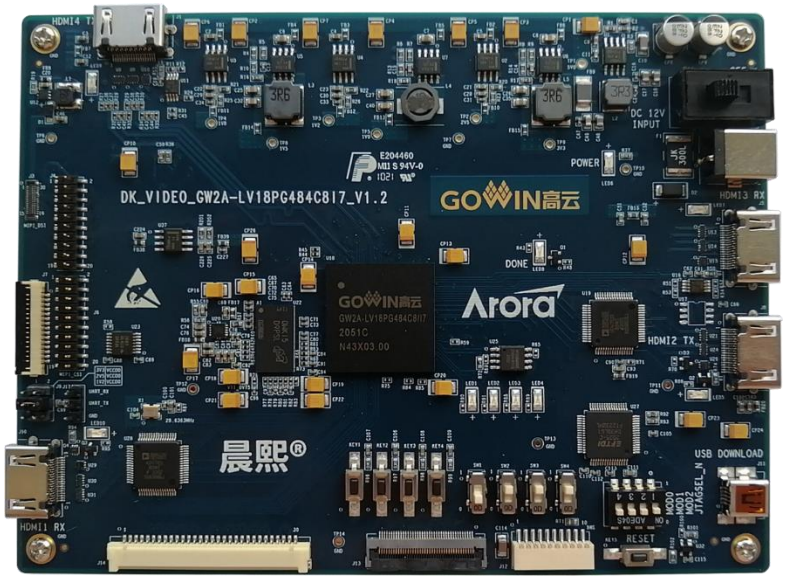
Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 Development Board Introduction

2.1 Overview

Figure 2-1 DK_VIDEO_GW2A-LV18PG484C8I7_V1.2 Development Board



DK_VIDEO_GW2A-LV18PG484C8I7_V1.2 development board applies to high-speed data storage based on DDR3, high-speed communication test based on LVDS and HDMI RX/TX, 18k series of FPGA evaluation, the hardware verification and software learning and debugging, etc.

The development board uses the GW2A-LV18PG484C8I7_V1.2 FPGA device, which is the first generation products of Gowin Arora family. The GW2A series of FPGA products offer a range of features and rich resources like high-performance DSP, high-speed LVDS interface and BSRAM. These embedded resources combine a streamlined FPGA architecture with a 55nm process to make the GW2A series of FPGA products ideal for high-speed and low-cost applications.

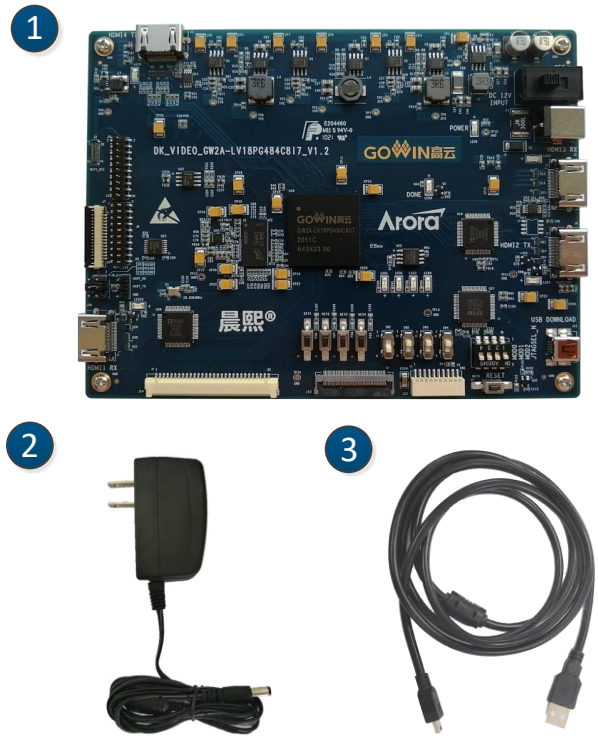
The development board includes a DDR3 chip with 2Gbit storage space and 16-bit data bus width. It integrates four HDMI interfaces, two of which are used to receive signals (One receives signals via decoding chip, and the other receives signals via FPGA IP), and the other two are used to transmit signals (One transmits signals via decoding chip, and the other transmits signals via FPGA IP). Besides that, this board also includes abundant external interfaces, including LVDS TX, LVDS RX, MIPI CSI, MIPI DSI, and GPIO. The external Flash is used to store FPGA configuration programs. Slide switches, keys, and LED facilitate users debugging.

2.2 A Development Kit

A development board kit includes the following items:

- DK_VIDEO_GW2A-LV18PG484C8I7_V1.2 development board
- 12V power (input: AC 100-240V~50/60Hz 25VA, output: DC 12V 2A)
- USB Mini B Cable

Figure 2-2 A Development Kit



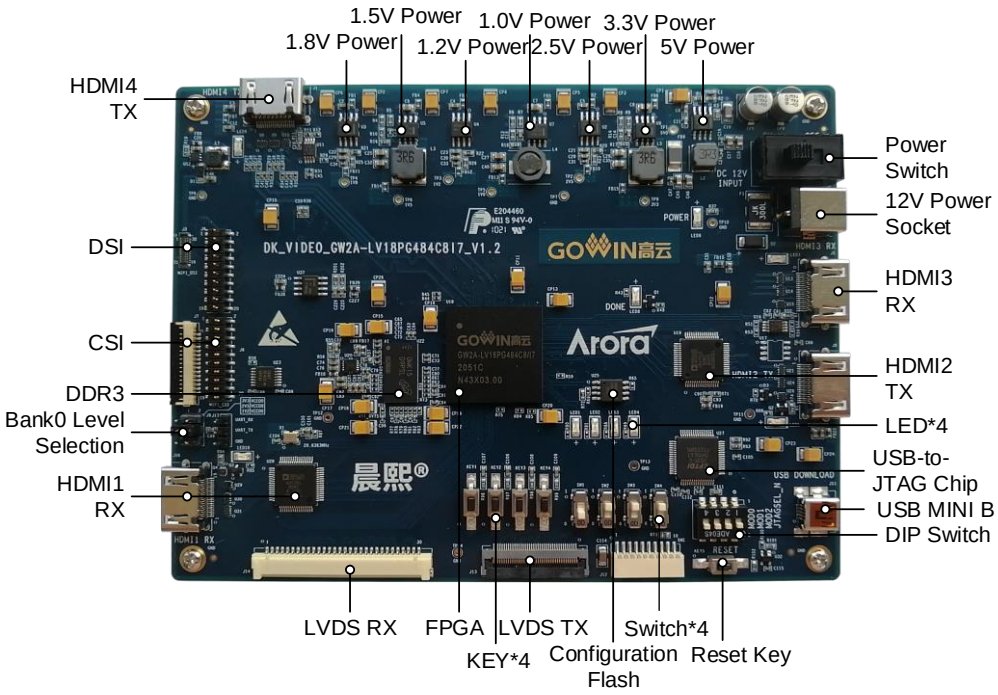
① DK_VIDEO_GW2A-LV18PG484C8I7_V1.2 development board

② 12V power supply

③ USB Mini B Cable

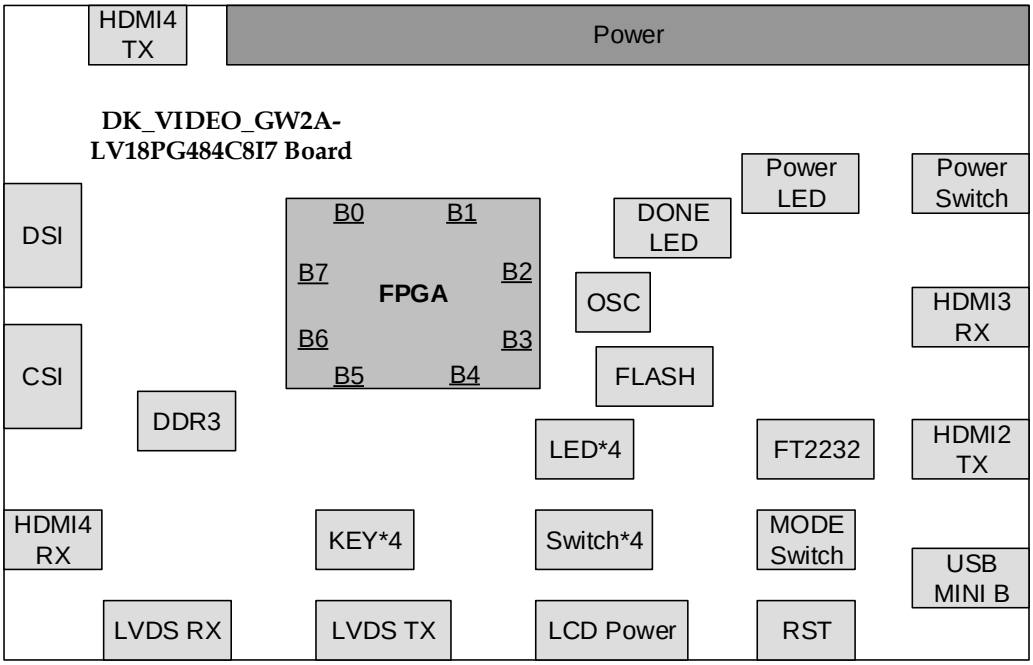
2.3 PCB Assembly

Figure 2-2 PCB Assembly



2.4 System Block Diagram

Figure 2-3 System Block Diagram



2.5 Features

The key features are as follows:

- The FPGA device
- Gowin GW2A-LV18PG484C8I7 FPGA
- Max. user I/O 319
- Download and Boot
- Integrates the download module and can be downloaded with the USB Mini B cable
- External Flash boot
- The blue DONE light is on after loading
- Power
- External DC 12V 2A
- The blue POWER light is on after power on
- The development board generates 5V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 1.0V, 0.75V and the power supply needed by LCD interface and MIPI interface
- Clock system 50MHz crystal oscillator
- Memory Device
- 2Gbit DDR3 SDRAM
- 64Mbit FLASH
- HDMI4 interfaces
- There are two HDMI inputs. One uses ADI ADV7611BSWZ chip and supports HDMI, DVI, and I2C interfaces with the maximum clock frequency of 165MHz. One connects to the FPGA pin directly and receive the HDMI signal via FPGA IP.
- There are two HDMI outputs. One uses ADI ADV7513BSWZ chip and supports HDMI, DVI, and I2C interfaces and the maximum clock frequency of 165MHz. One connects to the FPGA pin directly and transmit the HDMI signal via FPGA IP.

  Note!

  Bank0 voltage needs to be 2.5V when HDMI3 and HDMI4 are used.

- LVDS interfaces
- One LVDS interface for receiving, including ten pairs of differential signals
- One LVDS interface for transmitting, including ten pairs of differential signals
- MIPI DSI Interface
- The interface includes 5 pairs of differential signals, among which one for clock and four for data
- Stacked board connector with 30 contacts and 0.4mm pitch

- DSI signals of five lanes are simultaneously channeled to the double row pin of 20 pin and 2.00mm pitch

  Note!

  Bank0 voltage needs to be 1.2V if MIPI DSI is used.

- MIPI CSI Interface
- MIPI interface includes 3 pairs of differential signals, among which one for clock and four for data.
- 15pin FPC connector with 1mm pitch is used.
- Differential signals of three lanes are simultaneously channeled to the double row pin of 20 pin and 2.00mm pitch.

  Note!

  Bank0 voltage needs to be 1.2V if MIPI DSI is used.

- GPIO Interface

  The double row pin connected by MIPI interface can be reused as GPIO and differential output.

  Note!

  When used as GPIO and differential output, Bank voltage only supports 2.5V, and the terminating resistor needs to be removed to avoid affecting signal transmission.

- Debugging module
- Four keys
- Four switches
- Four blue LEDs

3 Development Board Circuit

3.1 FPGA Module

Overview

For the resources of GW2A-LV18PG484C8I7 FPGA Products, see DS102, *GW2A Series of FPGA Products Data Sheet*.

I/O BANK Introduction

For the I/O BANK, package, and pinout information, see UG111, GW2A Series of FPGA Products Package and Pinout User Guide.

3.2 Download Module

3.2.1 Introduction

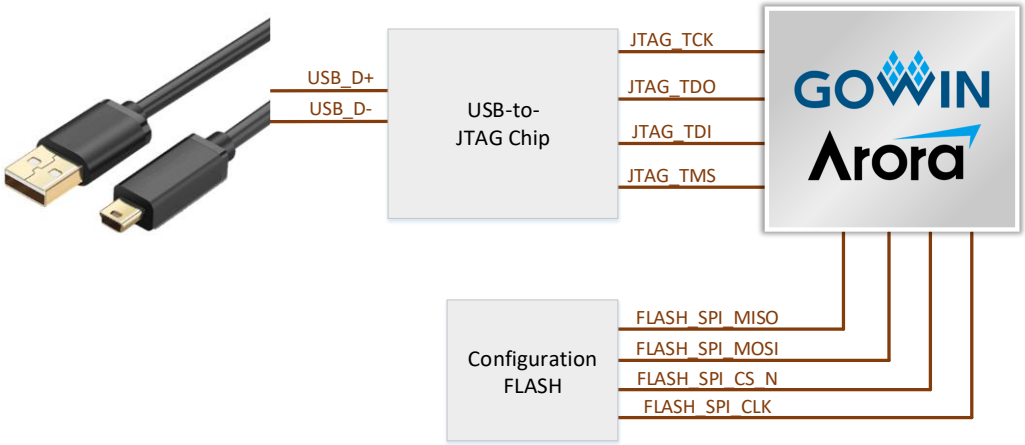
The development board provides USB download interface, which is realized by the A channel of FT2232 USB conversion chip. You can set the MODE value to download the programs to the on-chip SRAM or external Flash. When downloaded to SRAM, the data stream file will be lost if the device is power down. When downloaded to Flash, the data stream file will not be lost if power down.

The MODE value configuration is as follows:

- In any modes, you can download the data stream file to the on-chip SRAM and run it immediately.
- Set MODE as "011" to download the data stream file to the external Flash. Set MODE to "000" and power on again. The device will read the FPGA configuration data from the Flash automatically.

The connection diagram of downloading and configuration is as show in Figure 3-1.

Figure 3-1 FPGA Downloading and Configuration Connection Diagram



3.2.2 Pinout

Table 3-1 FPGA Download and Pinout

Name	FPGA Pin No.	BANK	I/O Level	Description
JTAG_TCK	N20	2	3.3V	JTAG Signal
JTAG_TDO	M22	2	3.3V	JTAG Signal
JTAG_TDI	M20	2	3.3V	JTAG Signal
JTAG_TMS	N22	2	3.3V	JTAG Signal
FLASH_SPI_MISO	P19	3	1.5V	FLASH signal configuration
FLASH_SPI_MOSI	P20	3	1.5V	FLASH signal configuration
FLASH_SPI_CS_N	N18	3	1.5V	FLASH signal configuration
FLASH_SPI_CLK	P18	3	1.5V	FLASH signal configuration

3.3 Power Supply

3.3.1 Introduction

The development board is powered via a power adapter. The input parameter is 100-240V~50/60MHz 25VA, and the output is DC +12V 2A.

The input 12V power can generate 5V, 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 1.0V and 0.75V power required by DDR3, 17.4V, +5V, and -5V required by MIPI DSI interface.

- One TPS54627 DC-DC power supply chip is used to generate 5V power, and the maximum output current is 6A;
- Three NCP3170ADR2G DC-DC power supply chips are used to

generate 3.3V, 1.5V, and 1.0V power, and the maximum output current is 3A.

- Three TPS7A7001 LDO power supply chips are used to generate 2.5V, 1.8V, and 1.2V, and the maximum output current is 2A.
- One TPS51200 power chip is used to generate 0.75v power for DDR3 chip.
- One AAT1541A power chip is used to generate +5V and -5v power for MIPI DSI interface.
- One TPS61161A power chip is used to generate 17.4v power for MIPI DSI interface backlighting.

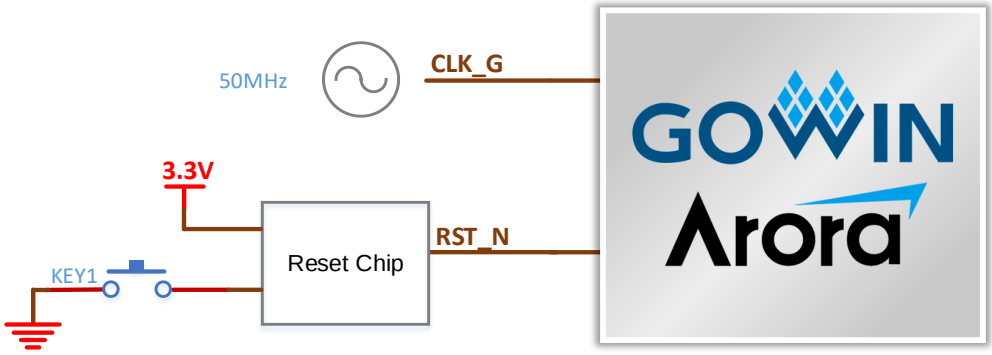
3.4 Clock and Reset

3.4.1 Introduction

The development board offers a 50MHz oscillator, connecting to the global clock pins.

The reset circuit uses keys and dedicated reset chips. After power on, the reset chip automatically generates a reset signal to reset the FPGA and Ethernet PHY chip. The 3.3V voltage is monitored in real time. The reset signal will be generated once an exception occurs. The reset signal can also be generated via the reset key.

Figure 3-2 Clock and Reset Connection Diagram



3.4.2 Pinout

Table 3-2 Clock and Reset Pinout

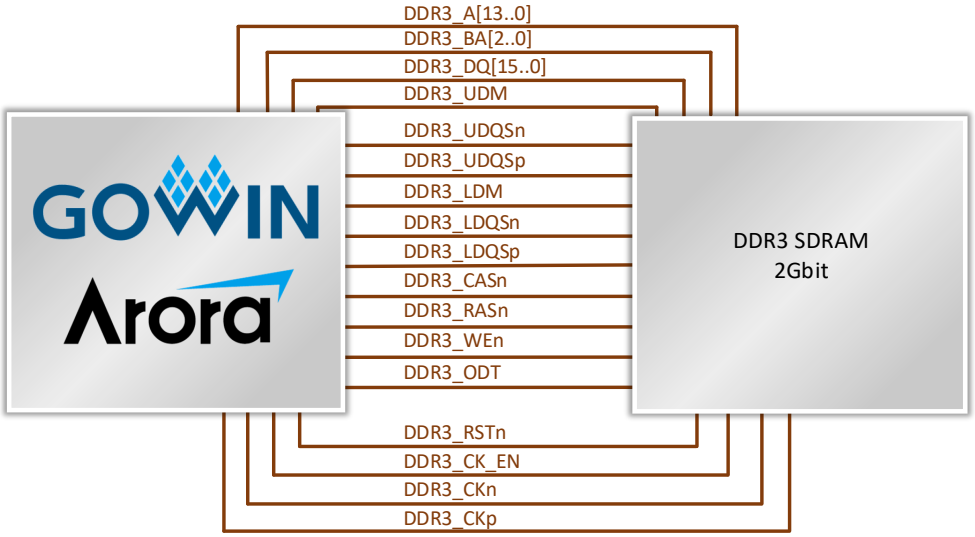
Name	FPGA Pin No.	BANK	I/O Level	Description
CLK_G	M19	2	3.3V	50MHz crystal oscillator input
RST_N	L22	2	3.3V	Reset Signal, active Low

3.5 DDR3

3.5.1 Introduction

The development board includes a DDR3 chip with 2Gbit storage space,16-bit data bus width, and a maximum data rate of 1600MT/s.

Figure 3-3 FPGA and DDR3 Connection Diagram



3.5.2 Pinout

Table 3-3 DDR3 Pinout

Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_A0	G1	7	1.5V	Address
DDR3_A1	U5	6	1.5V	Address
DDR3_A2	G5	7	1.5V	Address
DDR3_A3	F5	7	1.5V	Address
DDR3_A4	V3	6	1.5V	Address
DDR3_A5	G2	7	1.5V	Address
DDR3_A6	AA22	3	1.5V	Address
DDR3_A7	H5	7	1.5V	Address
DDR3_A8	AB22	3	1.5V	Address
DDR3_A9	J4	7	1.5V	Address
DDR3_A10	R5	6	1.5V	Address
DDR3_A11	AA21	3	1.5V	Address
DDR3_A12	T5	6	1.5V	Address
DDR3_A13	AA1	6	1.5V	Address

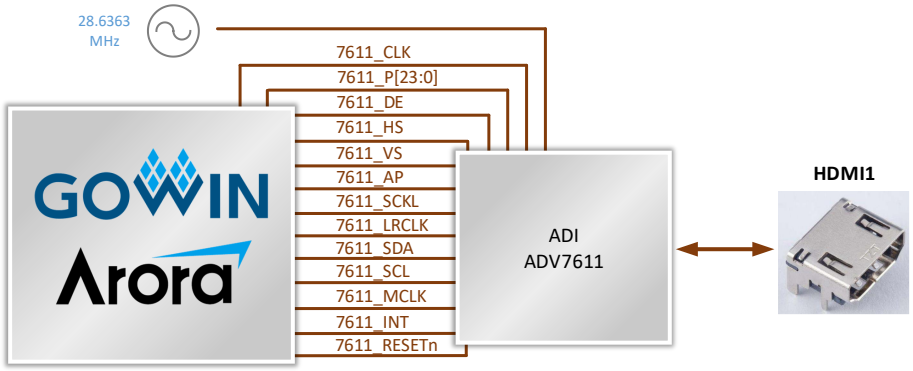
Name	FPGA Pin No.	BANK	I/O Level	Description
DDR3_BA0	F4	7	1.5V	Bank address
DDR3_BA1	U4	6	1.5V	Bank address
DDR3_BA2	F3	7	1.5V	Bank address
DDR3_CASn	C3	7	1.5V	Column address strobe
DDR3_CK_EN	E3	7	1.5V	Clock Enable
DDR3_CKn	R22	3	1.5V	Differential clock
DDR3_CKp	P22	3	1.5V	Differential clock
DDR3_DQ0	M5	6	1.5V	Data
DDR3_DQ1	T3	6	1.5V	Data
DDR3_DQ2	M3	6	1.5V	Data
DDR3_DQ3	T2	6	1.5V	Data
DDR3_DQ4	Y1	6	1.5V	Data
DDR3_DQ5	U1	6	1.5V	Data
DDR3_DQ6	N3	6	1.5V	Data
DDR3_DQ7	V1	6	1.5V	Data
DDR3_DQ8	T1	7	1.5V	Data
DDR3_DQ9	K3	7	1.5V	Data
DDR3_DQ10	P1	7	1.5V	Data
DDR3_DQ11	J1	7	1.5V	Data
DDR3_DQ12	L5	7	1.5V	Data
DDR3_DQ13	H3	7	1.5V	Data
DDR3_DQ14	M1	7	1.5V	Data
DDR3_DQ15	H1	7	1.5V	Data
DDR3_LDM	R3	6	1.5V	Data input mask
DDR3_LDQSn	R4	6	1.5V	Data strobe
DDR3_LDQSp	P4	6	1.5V	Data strobe
DDR3_ODT	B2	7	1.5V	On-Die Termination Enable
DDR3_RASn	D1	7	1.5V	Row address strobe
DDR3_RSTn	W4	6	1.5V	Reset
DDR3_UDM	K4	7	1.5V	Data input mask
DDR3_UDQSn	L1	7	1.5V	Data strobe
DDR3_UDQSp	L2	7	1.5V	Data strobe
DDR3_WEn	C1	7	1.5V	Write enable

3.6 HDMI1 Interface

3.6.1 Introduction

HDMI1 interface uses ADI decoding chip of ADV7611BSWZ, which is used to convert the input HDMI signal to RGB parallel data. The connection diagram is as shown below.

Figure 3-4 FPGA and HDMI1 Interface Connection Diagram



3.6.2 Pinout

Table 3-4 DDR3 Pinout

Name	FPGA Pin No.	BANK	I/O Level	Description
7611_CLK	W8	5	3.3V	The RGB data row locks the output clock
7611_P0	Y8	5	3.3V	RGB data signal
7611_P1	AB4	5	3.3V	RGB data signal
7611_P2	V9	5	3.3V	RGB data signal
7611_P3	AB5	5	3.3V	RGB data signal
7611_P4	Y10	5	3.3V	RGB data signal
7611_P5	U6	5	3.3V	RGB data signal
7611_P6	AB6	5	3.3V	RGB data signal
7611_P7	Y5	5	3.3V	RGB data signal
7611_P8	AA6	5	3.3V	RGB data signal
7611_P9	W6	5	3.3V	RGB data signal
7611_P10	AB7	5	3.3V	RGB data signal
7611_P11	Y6	5	3.3V	RGB data signal
7611_P12	AA7	5	3.3V	RGB data signal
7611_P13	V7	5	3.3V	RGB data signal
7611_P14	AB8	5	3.3V	RGB data signal

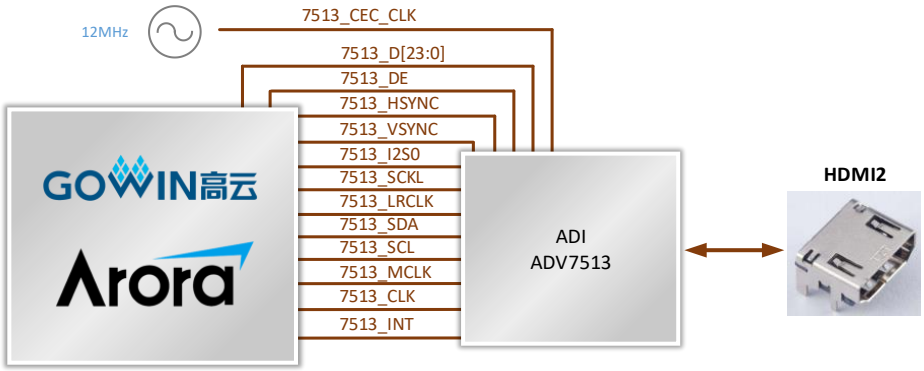
Name	FPGA Pin No.	BANK	I/O Level	Description
7611_P15	V8	5	3.3V	RGB data signal
7611_P16	Y9	5	3.3V	RGB data signal
7611_P17	AA8	5	3.3V	RGB data signal
7611_P18	W9	5	3.3V	RGB data signal
7611_P19	V10	5	3.3V	RGB data signal
7611_P20	AB10	5	3.3V	RGB data signal
7611_P21	W11	5	3.3V	RGB data signal
7611_P22	AA11	5	3.3V	RGB data signal
7611_P23	AB11	5	3.3V	RGB data signal
7611_VS	AB3	5	3.3V	Vertical Sync output signal
7611_HS	Y7	5	3.3V	Vertical Sync output signal
7611_DE	Y4	5	3.3V	RGB Data Enable
7611_SCLK	U7	5	3.3V	Audio Serial Clock
7611_LRCLK	AA3	5	3.3V	Audio left/right clock
7611_MCLK	V6	5	3.3V	Audio master clock
7611_AP	W7	5	3.3V	Audio output pin
7611_SCL	AB2	5	3.3V	I2C serial interface clock
7611_SDA	W5	5	3.3V	I2C serial interface data
7611_INT1	AB1	5	3.3V	Interrupt signal
7611_RESETn	Y3	5	3.3V	System Reset

3.7 HDMI2 Interface

3.7.1 Introduction

HDMI2 interface uses ADI decoding chip of ADV7513BSWZ, which is used to convert the FPGA output RGB parallel data to the HDMI signal. The connection diagram is as shown below.

Figure 3-5 FPGA and HDMI2 Interface Connection Diagram



3.7.2 Pinout

Table 3-5 DDR3 Pinout

Name	FPGA Pin No.	BANK	I/O Level	Description
7513_CLK	H21	2	3.3V	The RGB data row locks the output clock
7513_D0	K18	2	3.3V	RGB data signal
7513_D1	K19	2	3.3V	RGB data signal
7513_D2	J22	2	3.3V	RGB data signal
7513_D3	J19	2	3.3V	RGB data signal
7513_D4	J18	2	3.3V	RGB data signal
7513_D5	J20	2	3.3V	RGB data signal
7513_D6	H22	2	3.3V	RGB data signal
7513_D7	H19	2	3.3V	RGB data signal
7513_D8	H18	2	3.3V	RGB data signal
7513_D9	H20	2	3.3V	RGB data signal
7513_D10	G18	2	3.3V	RGB data signal
7513_D11	G19	2	3.3V	RGB data signal
7513_D12	G20	2	3.3V	RGB data signal
7513_D13	G22	2	3.3V	RGB data signal
7513_D14	F18	2	3.3V	RGB data signal
7513_D15	G21	2	3.3V	RGB data signal
7513_D16	F19	2	3.3V	RGB data signal
7513_D17	F20	2	3.3V	RGB data signal
7513_D18	F22	2	3.3V	RGB data signal
7513_D19	F21	2	3.3V	RGB data signal
7513_D20	E20	2	3.3V	RGB data signal
7513_D21	E22	2	3.3V	RGB data signal
7513_D22	E19	2	3.3V	RGB data signal
7513_D23	D20	2	3.3V	RGB data signal
7513_VSYNC	L19	2	3.3V	Vertical Sync output signal
7513_HSYNC	K22	2	3.3V	Vertical Sync output signal
7513_DE	K20	2	3.3V	RGB Data Enable
7513_SCLK	D17	1	2.5V	Audio Serial Clock
7513_LRCLK	D18	1	2.5V	Audio left/right clock
7513_MCLK	E17	1	2.5V	Audio master clock
7513_I2S0	C17	1	2.5V	Audio output pin

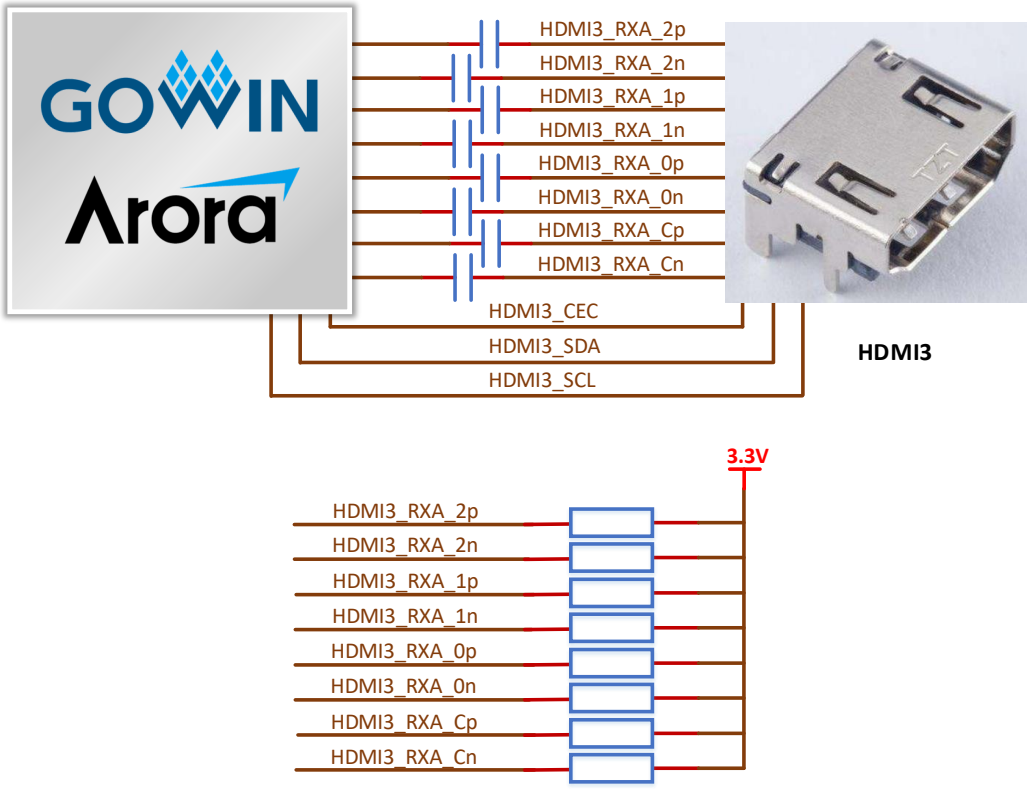
Name	FPGA Pin No.	BANK	I/O Level	Description
7513_SCL	A20	1	2.5V	I2C serial interface clock
7513_SDA	A21	1	2.5V	I2C serial interface data
7513_INT	L20	2	3.3V	Interrupt signal

3.8 HDMI3 Interface

3.8.1 Introduction

HDMI3 interface is connected to the FPGA pin directly. The HDMI signal is received via FPGA IP. The connection diagram is as shown below.

Figure 3-6 FPGA and HDMI3 Interface Connection Diagram



3.8.2 Pinout

Table 3-6 DDR3 Pinout

Name	FPGA Pin No.	BANK	I/O Level	Description
HDMI3_RX_Cp	C9	0	2.5V	HDMI differential clock
HDMI3_RX_Cn	C10	0	2.5V	HDMI differential clock
HDMI3_RX_0p	C7	0	2.5V	HDMI differential data
HDMI3_RX_0n	C8	0	2.5V	HDMI differential data
HDMI3_RX_1p	D5	0	2.5V	HDMI differential data

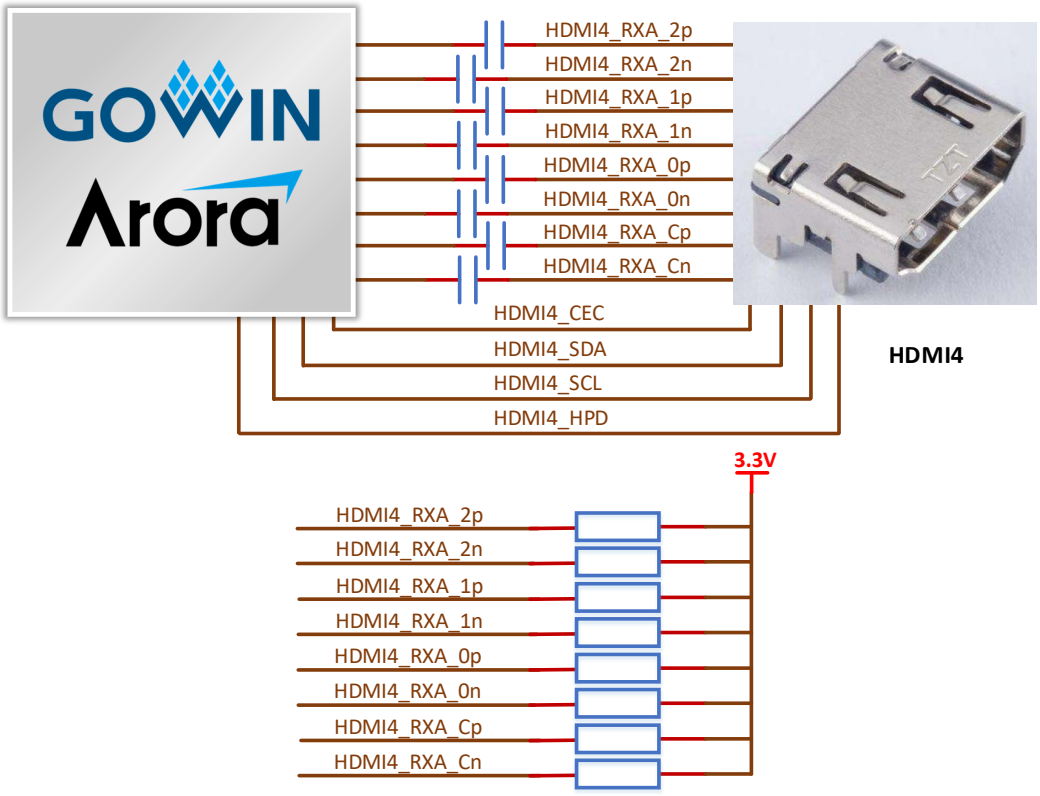
Name	FPGA Pin No.	BANK	I/O Level	Description
HDMI3_RX_1n	D6	0	2.5V	HDMI differential data
HDMI3_RX_2p	D4	0	2.5V	HDMI differential data
HDMI3_RX_2n	C4	0	2.5V	HDMI differential data
HDMI3_CEC	C22	2	3.3V	Consumer electronic control signals
HDMI3_SCL	D22	2	3.3V	I2C serial clock
HDMI3_SDA	C21	2	3.3V	I2C serial data

3.9 HDMI4 Interface

3.9.1 Introduction

HDMI4 interface is connected to the FPGA pin directly. The HDMI signal is transmitted via FPGA IP. The connection diagram is as shown below.

Figure 3-7 FPGA and HDMI4 Connection Diagram



3.9.2 Pinout

Table 3-7 DDR3 Pinout

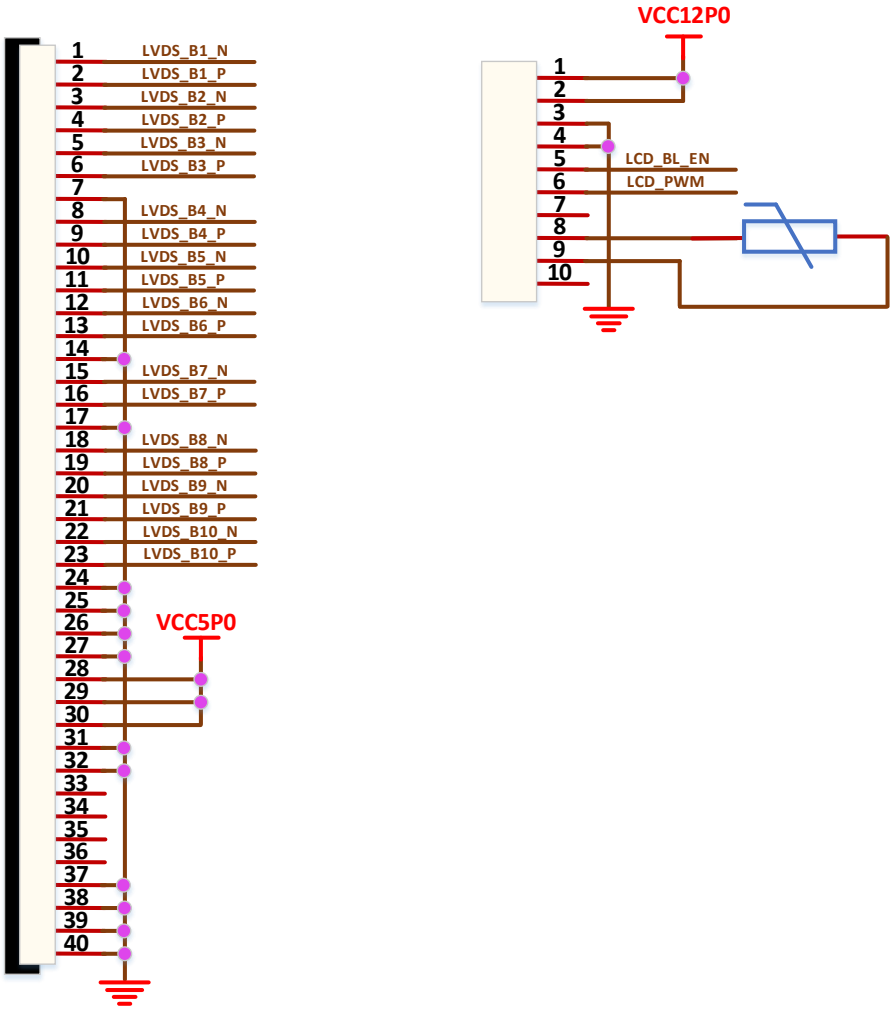
Name	FPGA Pin No.	BANK	I/O Level	Description
HDMI4_TX_Cp	A11	0	2.5V	HDMI differential clock
HDMI4_TX_Cn	A12	0	2.5V	HDMI differential clock
HDMI4_TX_0p	A9	0	2.5V	HDMI differential data
HDMI4_TX_0n	A10	0	2.5V	HDMI differential data
HDMI4_TX_1p	B6	0	2.5V	HDMI differential data
HDMI4_TX_1n	A6	0	2.5V	HDMI differential data
HDMI4_TX_2p	A2	0	2.5V	HDMI differential data
HDMI4_TX_2n	A3	0	2.5V	HDMI differential data
HDMI4_HPD	B21	2	3.3V	Hot Plug Detect
HDMI4_CEC	B20	2	3.3V	Consumer electronic control signals
HDMI4_SCL	D19	2	3.3V	I2C serial clock
HDMI4_SDA	C20	2	3.3V	I2C serial data

3.10 LVDS TX Interface

3.10.1 Introduction

LVDS TX interface connects to ten pairs of differential signal, including eight pairs of data and two pairs of clock. The interface supports the screen of Xinli TFT19201080-30-E. 40pin FPC connector with 0.5mm pitch is used. When connected to the LCD screen, the LED backlighting is powered and controlled via a separate power supply interface.

Figure 3-8 LVDS TX Interface Diagram



3.10.2 Pinout

Table 3-8 LVDS TX Interface Pinout

Name	FPGA Pin No.	BANK	I/O Level	Description
LVDS_B1_N	U16	4	2.5V	Differential Channel 1-
LVDS_B1_P	V16	4	2.5V	Differential Channel 1+
LVDS_B2_N	V18	4	2.5V	Differential Channel 1-
LVDS_B2_P	V17	4	2.5V	Differential Channel 1+
LVDS_B3_N	Y18	4	2.5V	Differential Channel 1-
LVDS_B3_P	Y19	4	2.5V	Differential Channel 1+
LVDS_B4_N	Y17	4	2.5V	Differential Channel 1-
LVDS_B4_P	AA17	4	2.5V	Differential Channel 1+
LVDS_B5_N	AA16	4	2.5V	Differential Channel 1-
LVDS_B5_P	AB16	4	2.5V	Differential Channel 1+
LVDS_B6_N	AA15	4	2.5V	Differential Channel 1-
LVDS_B6_P	AB15	4	2.5V	Differential Channel 1+

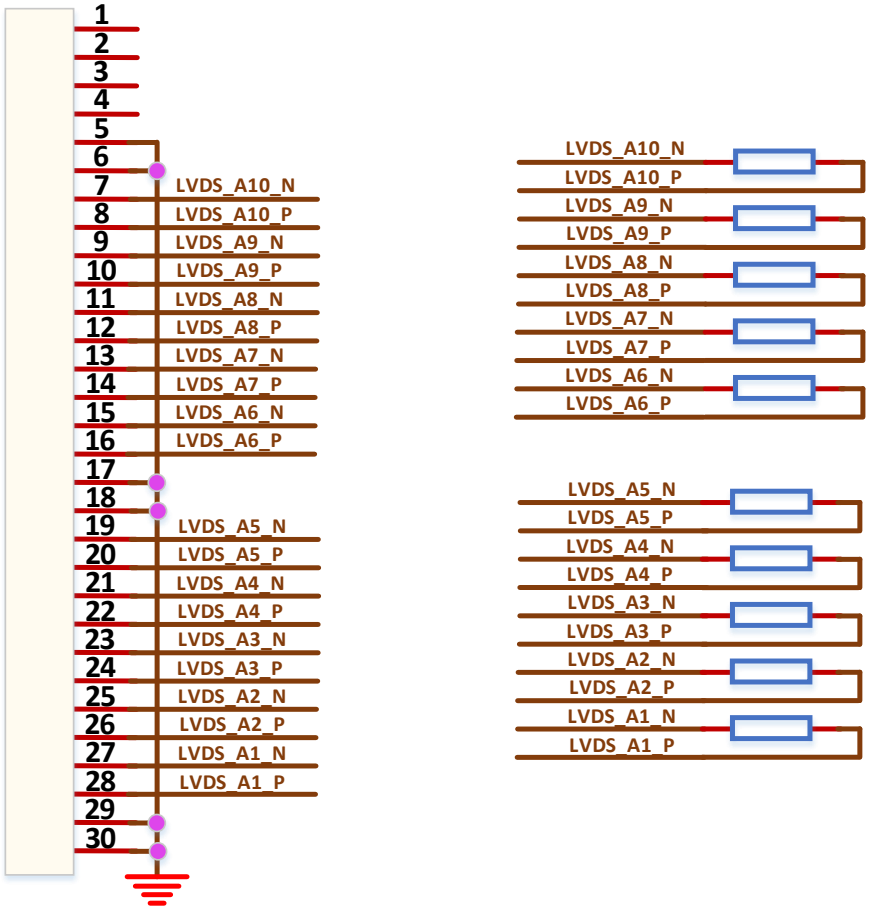
Name	FPGA Pin No.	BANK	I/O Level	Description
LVDS_B7_N	W16	4	2.5V	Differential Channel 1-
LVDS_B7_P	Y16	4	2.5V	Differential Channel 1+
LVDS_B8_N	V15	4	2.5V	Differential Channel 1-
LVDS_B8_P	V14	4	2.5V	Differential Channel 1+
LVDS_B9_N	AA12	4	2.5V	Differential Channel 1-
LVDS_B9_P	AB12	4	2.5V	Differential Channel 1+
LVDS_B10_N	W13	4	2.5V	Differential Channel 1-
LVDS_B10_P	W12	4	2.5V	Differential Channel 1+
LCD_BL_EN	M21	2	3.3V	Backlight enable
LCD_PWM	L21	2	3.3V	Backlighting PWM

3.11 LVDS RX Interface

3.11.1 Introduction

LVDS RX interface connects to ten pairs of differential signal, including eight pairs of data and two pairs of clock. The interface uses 30pin FPC connector with the pitch of 1.25mm.

Figure 3-9 LVDS RX Interface Diagram



3.11.2 Pinout

Table 3-9 LVDS RX Interface Pinout

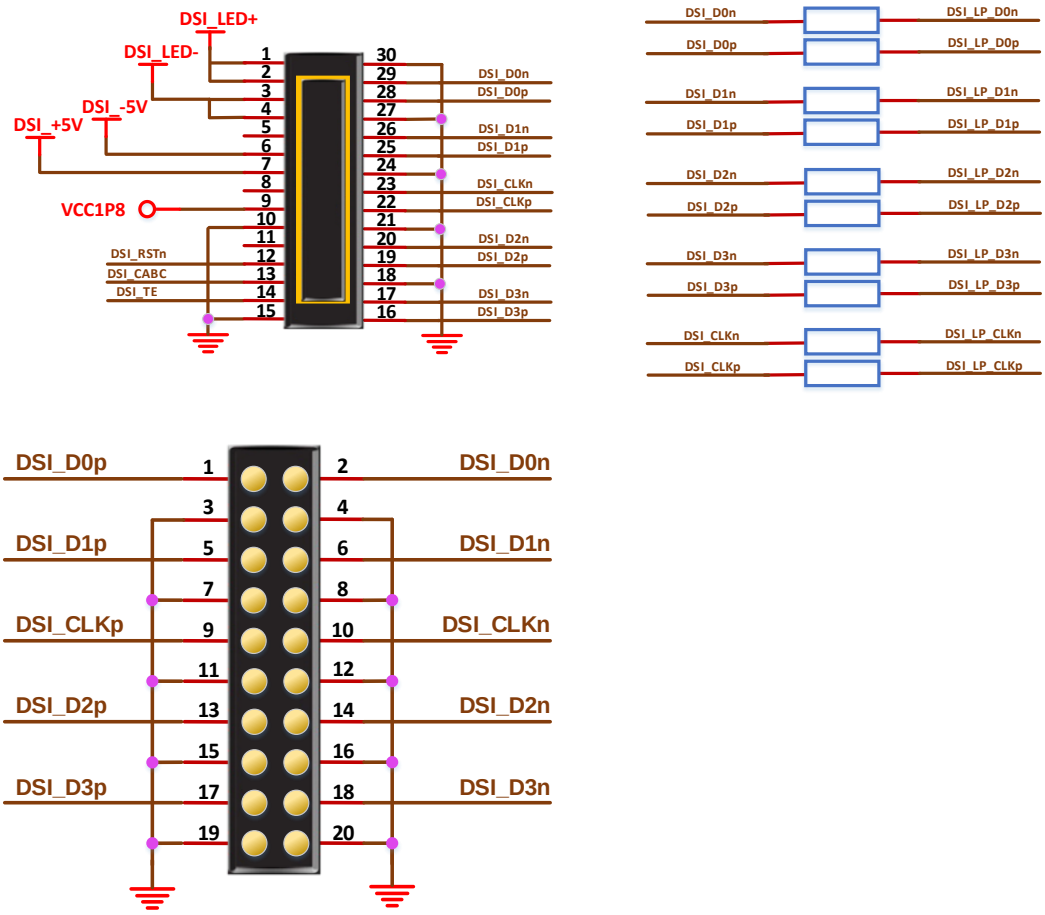
Name	FPGA Pin No.	BANK	I/O Level	Description
LVDS_A1_N	V19	4	2.5V	Differential Channel 1-
LVDS_A1_P	W19	4	2.5V	Differential Channel 1+
LVDS_A2_N	W18	4	2.5V	Differential Channel 1-
LVDS_A2_P	W17	4	2.5V	Differential Channel 1+
LVDS_A3_N	AB20	4	2.5V	Differential Channel 1-
LVDS_A3_P	AB19	4	2.5V	Differential Channel 1+
LVDS_A4_N	Y20	4	2.5V	Differential Channel 1-
LVDS_A4_P	AA20	4	2.5V	Differential Channel 1+
LVDS_A5_N	AB18	4	2.5V	Differential Channel 1-
LVDS_A5_P	AB17	4	2.5V	Differential Channel 1+
LVDS_A6_N	Y15	4	2.5V	Differential Channel 1-
LVDS_A6_P	Y14	4	2.5V	Differential Channel 1+
LVDS_A7_N	W15	4	2.5V	Differential Channel 1-
LVDS_A7_P	W14	4	2.5V	Differential Channel 1+
LVDS_A8_N	AB14	4	2.5V	Differential Channel 1-
LVDS_A8_P	AB13	4	2.5V	Differential Channel 1+
LVDS_A9_N	Y13	4	2.5V	Differential Channel 1-
LVDS_A9_P	Y12	4	2.5V	Differential Channel 1+
LVDS_A10_N	V13	4	2.5V	Differential Channel 1-
LVDS_A10_P	V12	4	2.5V	Differential Channel 1+

3.12 MIPI DSI

3.12.1 Introduction

The DSI interface uses the 30-contact stacked board connector, which channels to 5 pairs of differential signals, including one for clock and four for data, corresponding to TXD T550UZPA-75 mobile phone screen interface. At the same time, DSI signals of 5 lanes are channeled to the double rows pin of 20pin with 2.00mm pitch.

Figure 3-10 MIPI DSI Connection Diagram



3.12.2 Pinout

Table 3-10 MIPI DSI Interface Pinout

Name	FPGA Pin No.	BANK	I/O Level	Description
DSI_D0n	B22	1	2.5V	HS differential data 0-
DSI_D0p	A22	1	2.5V	HS differential data 0+
DSI_D1n	C19	1	2.5V	HS differential data 1-
DSI_D1p	C18	1	2.5V	HS differential data 1+
DSI_CLKn	A19	1	2.5V	HS Differential clock-
DSI_CLKp	A18	1	2.5V	HS Differential clock+
DSI_D2n	B17	1	2.5V	HS differential data 2-
DSI_D2p	A17	1	2.5V	HS differential data 2+
DSI_D3n	B15	1	2.5V	HS differential data 3-
DSI_D3p	A15	1	2.5V	HS differential data 3+
DSI_LP_D0n	E7	0	1.2V	LP single port data 0
DSI_LP_D0p	B11	0	1.2V	LP single port data 0
DSI_LP_D1n	B8	0	1.2V	LP single port data 1

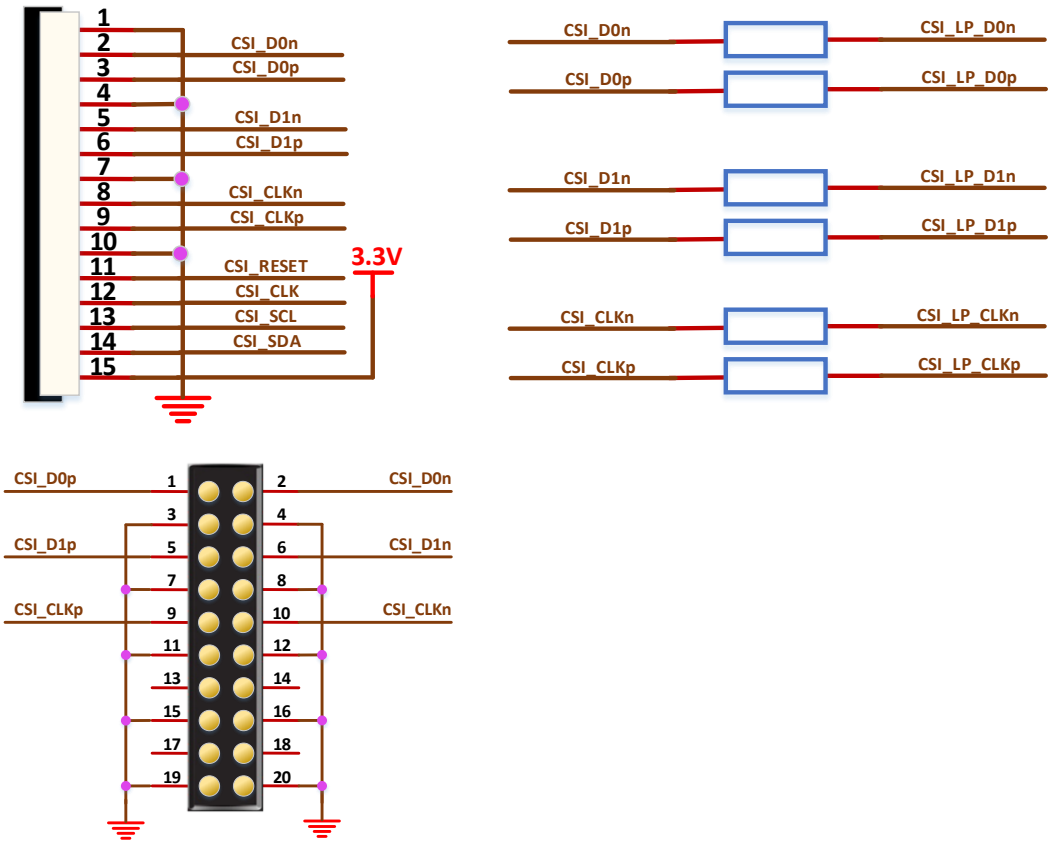
Name	FPGA Pin No.	BANK	I/O Level	Description
DSI_LP_D1p	A8	0	1.2V	LP single port data 1
DSI_LP_CLKn	B7	0	1.2V	LP single port clock
DSI_LP_CLKp	A7	0	1.2V	LP single port clock
DSI_LP_D2n	C6	0	1.2V	LP single port data 2
DSI_LP_D2p	D7	0	1.2V	LP single port data 2
DSI_LP_D3n	D8	0	1.2V	LP single port data 3
DSI_LP_D3p	D9	0	1.2V	LP single port data 3
DSI_RSTn	A16	1	2.5V	Reset signal
DSI_CABC	B16	1	2.5V	Backlighting control signal
DSI_TE	D16	1	2.5V	Tearing effect output signal

3.13 MIPI CSI

3.13.1 Introduction

MIPI CSI uses 15pin connector with 1mm pitch. The interface includes 3 pairs of differential signals, among which one for clock and two for data. Differential signals of three lanes are simultaneously channeled to the double rows pin of 20 pin with 2.00mm pitch.

Figure 3-11 MIPI CSI Connection Diagram



3.13.2 Pinout

Table 3-11 MIPI DSI Interface Pinout

Name	FPGA Pin No.	BANK	I/O Level	Description
CSI_D0n	C15	1	2.5V	HS differential data 0-
CSI_D0p	C14	1	2.5V	HS differential data 0+
CSI_D1n	E13	1	2.5V	HS differential data 1-
CSI_D1p	E12	1	2.5V	HS differential data 1+
CSI_CLKn	D12	1	2.5V	HS Differential clock-
CSI_CLKp	D11	1	2.5V	HS Differential clock+
CSI_LP_D0n	E6	0	1.2V	LP single port data 0
CSI_LP_D0p	A5	0	1.2V	LP single port data 0
CSI_LP_D1n	A1	0	1.2V	LP single port data 1
CSI_LP_D1p	B1	0	1.2V	LP single port data 1
CSI_LP_CLKn	A4	0	1.2V	LP single port clock
CSI_LP_CLKp	C5	0	1.2V	LP single port clock
F_CSI_RESET	E16	1	2.5V	Reset signal
F_CSI_CLK	C16	1	2.5V	Clock
F_CSI_SCL	D15	1	2.5V	I2C signal
F_CSI_SDA	E15	1	2.5V	I2C signal

3.14 GPIO

3.14.1 Introduction

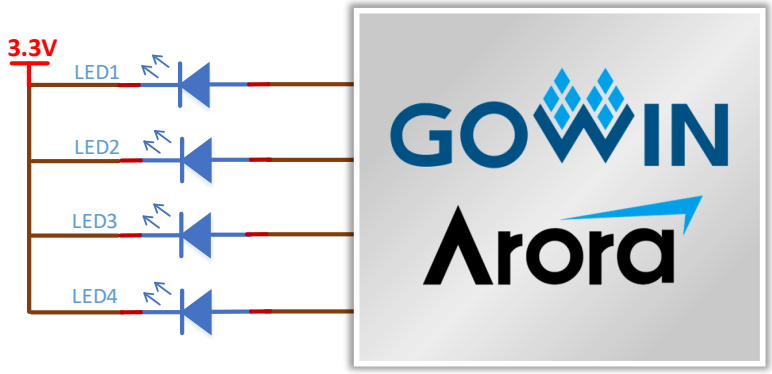
The double rows pins of MIPI DSI and MIPI CSI on the development board can be reused as GPIO when they are not in use. Due to their connection to the termination resistor of FPGA and LP simultaneously, users need to remove the termination resistor and Bank voltage needs to be 2.5V when the double rows pins are reused as GPIO. For the diagram and pins distribution, refer to 3.12 MIPI DSI and 3.13 MIPI CSI.

3.15 LED Module

3.15.1 Introduction

There are four blue LED lights on the development board, which can be used to display status. When the output signal of FPGA corresponding pin is low, the LED is lit up. When the output signal is high, the LED is off. The diagram is as shown in Figure 3-12.

Figure 3-12 LED Connection Diagram



3.15.2 Pinout

Table 3-12 LED Pinout

Name	FPGA Pin No.	BANK	I/O Level	Description
LED1	W20	3	1.5V	LED1
LED2	W22	3	1.5V	LED2
LED3	V22	3	1.5V	LED3
LED4	U20	3	1.5V	LED4

Note!

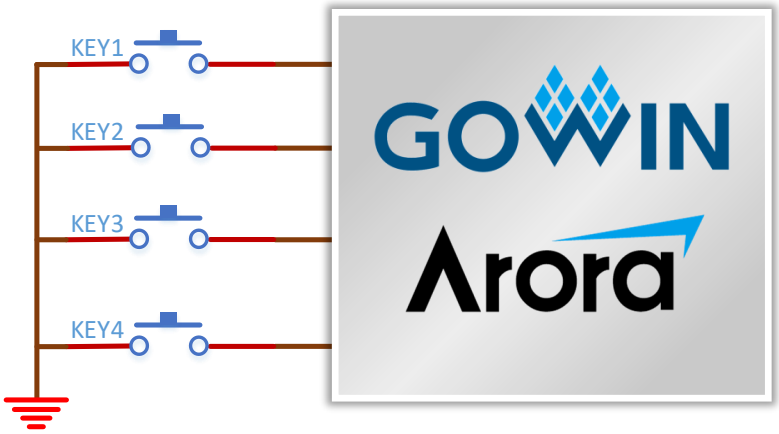
SSPI needs to be reused as GPIO.

3.16 Keys Module

3.16.1 Introduction

The development board has four keys that can be used to control input during testing. When the key is pressed, the input is low. The diagram is as shown in Figure 3-13.

Figure 3-13 Key Circuit Diagram



3.16.2 Pinout

Table 3-13 Keys Module Pinout

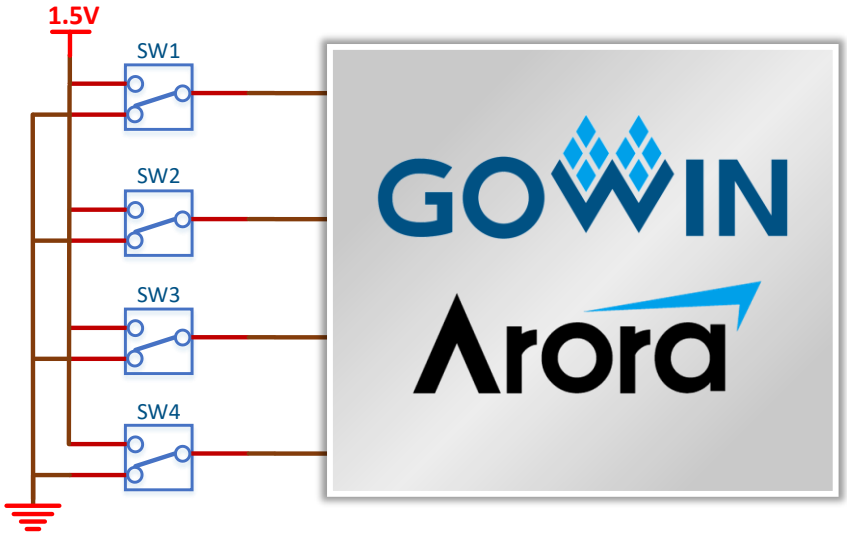
Name	FPGA Pin No.	BANK	I/O Level	Description
KEY1	AB21	3	1.5V	KEY1
KEY2	Y21	3	1.5V	KEY2
KEY3	U18	3	1.5V	KEY3
KEY4	V20	3	1.5V	KEY4

3.17 Switches Module

3.17.1 Introduction

There are four slide switches on the development board to control input during testing.

Figure 3-14 Switch Circuit Diagram



3.17.2 Pinout

Table 3-14 Switches Module Pinout

Name	FPGA Pin No.	BANK	I/O Level	Description
SW1	T17	3	1.5V	Slide switch1
SW2	T18	3	1.5V	Slide switch2
SW3	R18	3	1.5V	Slide switch3
SW4	R19	3	1.5V	Slide switch4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